

# PCA9703

18 V tolerant SPI 16-bit GPI with maskable  $\overline{\text{INT}}$

Rev. 4 — 5 September 2014

Product data sheet

## 1. General description

---

The PCA9703 is a low power 18 V tolerant SPI General Purpose Input (GPI) shift register designed to monitor the status of switch inputs. It generates an interrupt when one or more of the switch inputs change state but allows selected inputs to not generate interrupts using the interrupt masking feature. The input level is recognized as a HIGH when it is greater than  $0.8 \times V_{\text{DD}}$  and as a LOW when it is less than  $0.55 \times V_{\text{DD}}$  (minimum LOW threshold of 2.5 V at 5 V node). The PCA9703 can monitor up to 16 switch inputs.

The falling edge of the  $\overline{\text{CS}}$  pin samples the input port status and clears the interrupt. When  $\overline{\text{CS}}$  is LOW, the rising edge of the SCLK loads the shift register and shifts the value out of the shift register. The serial input is sampled on the falling edge of SCLK. The contents of the shift register are loaded into the interrupt mask register of the device on the rising edge of  $\overline{\text{CS}}$ .

Each of the input ports has a 18 V breakdown ESD protection circuit, which dumps the ESD/overvoltage current to ground. When used with a series resistor (minimum 100 k $\Omega$ ), the input can connect to a 12 V battery and support double battery, reverse battery, 27 V jump start and 40 V load dump conditions in automotive applications. Higher voltages can be tolerated on the inputs depending on the series resistor used to limit the input current.

The INT\_EN pin is used to both enable the GPI pins and to enable the  $\overline{\text{INT}}$  output pin to minimize battery drain in cyclically supplied pull-up or pull-down applications. The SDIN pull-down prevents floating nodes when the device is used in daisy-chain applications.

With both the high breakdown voltage and high ESD, this device is useful for both automotive (AEC-Q100 compliance available) and mobile applications.

## 2. Features and benefits

---

- 16 general purpose input ports
- 18 V tolerant input ports with 100 k $\Omega$  external series resistor
- Input LOW threshold  $0.55 \times V_{\text{DD}}$  with minimum of 2.5 V at  $V_{\text{DD}} = 4.5 \text{ V}$
- Open-drain interrupt output
- Interrupt enable pin (INT\_EN) disables GPI pins and interrupt output
- Interrupt-masking feature allows no interrupt generation from selected inputs
- $V_{\text{DD}}$  range: 4.5 V to 5.5 V
- $I_{\text{DD}}$  is very low 2.5  $\mu\text{A}$  maximum
- SPI serial interface with speeds up to 5 MHz
- SPI supports daisy-chain connection for large switch numbers
- AEC-Q100 compliance available



- ESD protection exceeds 5 kV HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: -40 °C to +125 °C
- Offered in TSSOP24 and HWQFN24 packages

### 3. Applications

- Automotive
  - ◆ Body control modules
  - ◆ Electronic control units (for example, for body controller)
  - ◆ Switch monitoring
  - ◆ SBC wake pin extension
- Industrial equipment
- Cellular telephones
- Emergency lighting

### 4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9703HF	9703	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1
PCA9703PW	PCA9703PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9703PW/Q900 <sup>[1]</sup>	PCA9703PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] PCA9703PW/Q900 is AEC-Q100 compliant. Contact [i2c.support@nxp.com](mailto:i2c.support@nxp.com) for PPAP.

### 5. Block diagram

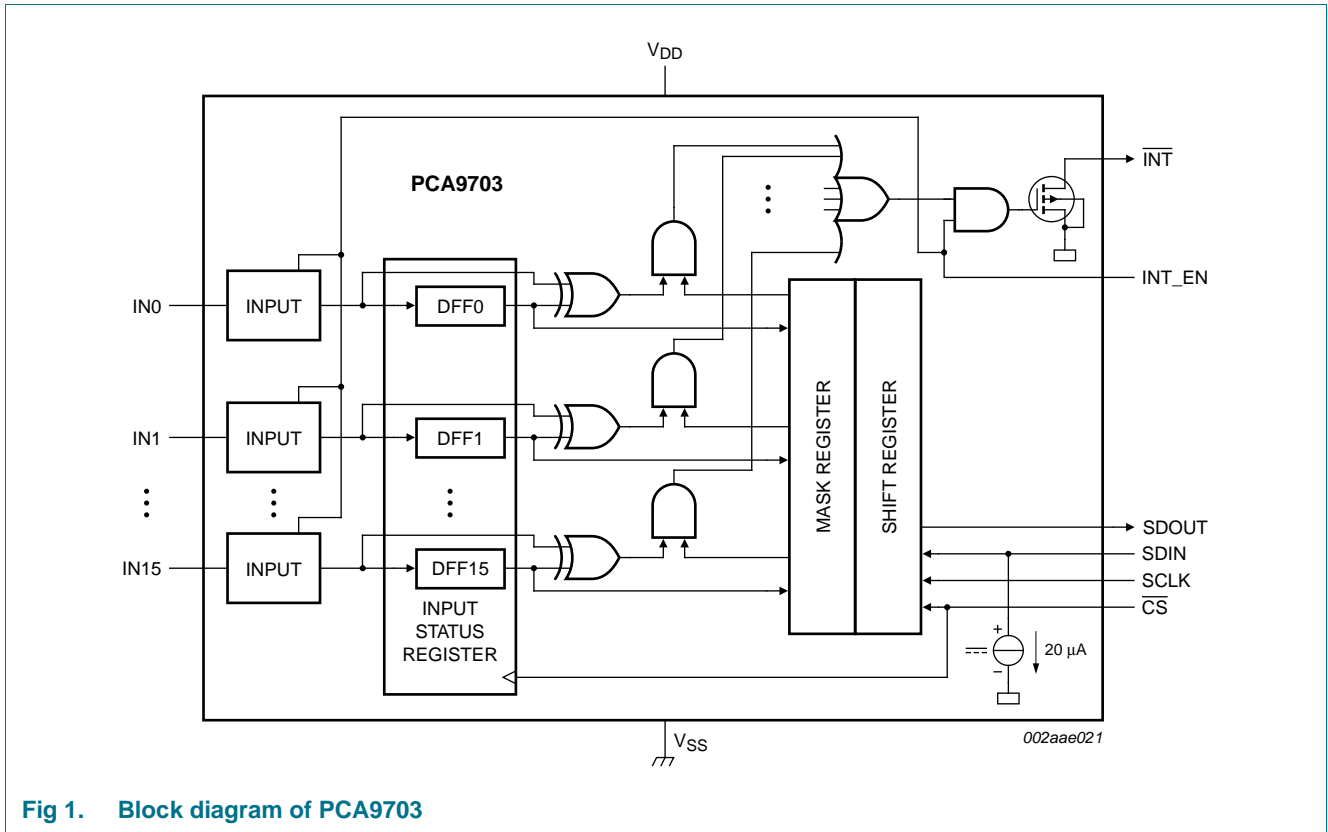


Fig 1. Block diagram of PCA9703

### 6. Pinning information

#### 6.1 Pinning

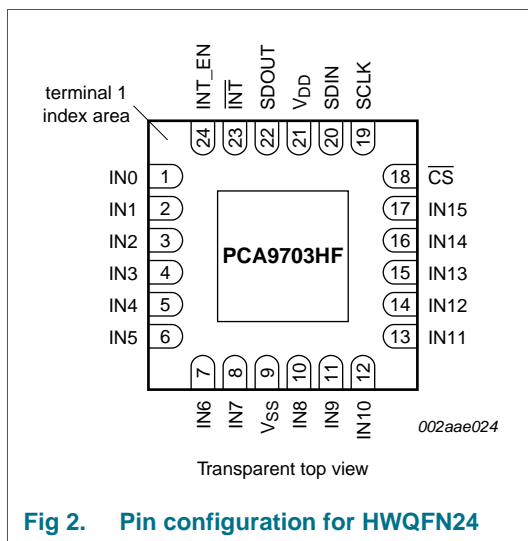


Fig 2. Pin configuration for HWQFN24

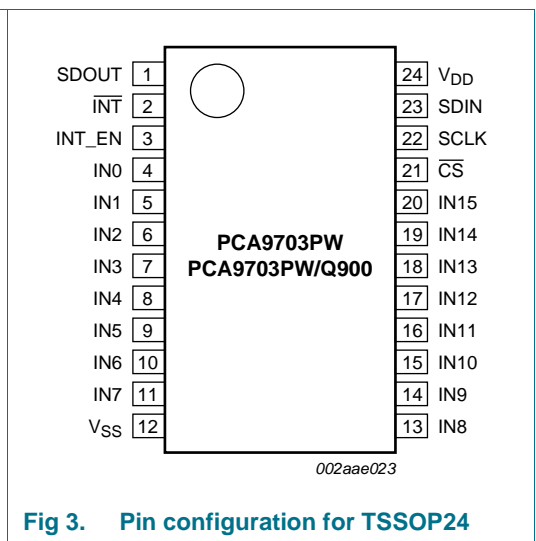


Fig 3. Pin configuration for TSSOP24

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	TSSOP24	HWQFN24		
SDOUT	1	22	output	3-state serial data output; normally high-impedance
$\overline{\text{INT}}$	2	23	output	open-drain interrupt output (active LOW)
INT_EN	3	24	input	GPI pin enable and interrupt output enable 1 = GPI pin and interrupt output are enabled 0 = GPI pin and interrupt output are disabled and interrupt output is high-impedance
IN0	4	1	input	input port 0
IN1	5	2	input	input port 1
IN2	6	3	input	input port 2
IN3	7	4	input	input port 3
IN4	8	5	input	input port 4
IN5	9	6	input	input port 5
IN6	10	7	input	input port 6
IN7	11	8	input	input port 7
V <sub>SS</sub>	12	9 <sup>[1]</sup>	ground	ground supply
IN8	13	10	input	input port 8
IN9	14	11	input	input port 9
IN10	15	12	input	input port 10
IN11	16	13	input	input port 11
IN12	17	14	input	input port 12
IN13	18	15	input	input port 13
IN14	19	16	input	input port 14
IN15	20	17	input	input port 15
$\overline{\text{CS}}$	21	18	input	chip select (active LOW)
SCLK	22	19	input	serial input clock
SDIN	23	20	input	serial data input (20 $\mu$ A pull-down)
V <sub>DD</sub>	24	21	supply	supply voltage

- [1] HWQFN24 package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

## 7. Functional description

PCA9703 is a 16-bit General Purpose Input (GPI) with an open-drain interrupt output designed to monitor switch status. By putting an external 100 k $\Omega$  series resistor at the input port, the device allows the input to tolerate momentary double 12 V battery, reverse battery, 27 V jump start or 40 V load dump conditions. The interrupt output is asserted when an input port status changes, the input is not masked and the interrupt output is enabled. The open-drain interrupt output is enabled when INT\_EN is HIGH and disabled when INT\_EN is LOW. The INT\_EN also enables the GPI pins when it is HIGH. In cyclically supplied pull-up or pull-down applications, the GPI pull-ups or pull-downs should be active before the INT\_EN is taken HIGH and the INT output should only be sampled after transient conditions have settled. Additionally, interrupts can be disabled in software by using the interrupt mask feature. The input port status is accessed via the 4-wire SPI interface.

Upon power-up, the power-up reset cell clears all the registers, resulting in all zeros in both the input status register and the interrupt mask register. Since a zero in the interrupt mask register masks the interrupt from that pin, there will not be any interrupts generated. After power-up it is necessary to access the PCA9703 through the SPI pins in order to activate the interrupt for any GPI pins. When the PCA9703 is read over the SPI wires, the input conditions are clocked into the input status register on the  $\overline{CS}$  falling edge. Since the inputs and the input status register now match, no interrupt is generated and any pre-existing interrupt is cleared. The input status register data is parallel loaded into the shift register on the first rising edge of the SCLK. The serial input data is captured on the opposite clock edge so that there is a  $\frac{1}{2}$  clock cycle hold time. The set-up time is diminished by the propagation time so the SCLK falling edge to rising edge must be long enough to provide sufficient set-up time. Successive clock cycles on the SCLK pin clock the data out of the PCA9703 and new data from the SDIN into the shift register. There is no limit to the number of clock cycles that can be applied with the  $\overline{CS}$  LOW, however sufficient clock cycles should be used to both shift out all of the GPI data and shift in the new interrupt mask data to the correct position with the MSB first before the  $\overline{CS}$  rising edge.

For cyclic switch bias applications the switch bias should be applied first, then after the input voltage is settled the general purpose inputs are switched on by taking the INT\_EN HIGH. This also enables the interrupt output, which will only indicate an interrupt if the GPI data does not match the input status register on a bit that is enabled by the interrupt mask register value. If an interrupt is generated, the pull-up or pull-down source should remain active and the INT\_EN should remain active and the SPI pins are used to update the input status register and read the data out. They are also used to store the new interrupt mask on the rising edge of  $\overline{CS}$ . After the SPI transaction is complete the INT\_EN is taken LOW to turn the inputs off and disable the  $\overline{INT}$  output. Then the GPI pull-ups or pull-downs can be turned off. The GPI pins are specifically designed so that any ESD/overstress current flows to ground, not  $V_{DD}$ . They are also specifically designed so that if the input voltage returns to the same value after pull-up or pull-down bias cycling as before the input pull-up or pull-down bias cycling, before the input is enabled it will be detected as the same state. If the Input Status register is read when INT\_EN is LOW, the input state at the INT\_EN transition will be output regardless of the actual input levels since the GPI pins are turned off.

If the  $V_{DD}$  falls below the 4.5 V minimum specified supply voltage, the input threshold will move down since they are a function of the  $V_{DD}$  voltage. The input status register and the interrupt mask register retain their values to below  $V_{DD} = 2.0$  V and power-down can only be used to generate a power-up reset if the  $V_{DD}$  falls below 0.2 V before returning to the operating range.

Multiple PCA9703 devices can be serially connected for monitoring a large number of switches by connecting the SDO $\overline{U}$ T of one device to the SDIN of the next device. SCLK and  $\overline{CS}$  must be common among all devices and interrupt outputs may be tied together. No external logic is necessary because all the devices' interrupt outputs are open-drain that function as 'wired-AND' and can simply be connected together to a single pull-up resistor.

## 7.1 SPI bus operation

The PCA9703 interfaces with the controller via the 4-wire SPI bus that is comprised of the following signals: chip select ( $\overline{CS}$ ), serial clock (SCLK), serial data in (SDIN), and serial data out (SDOUT). To access the device, the controller asserts  $\overline{CS}$  LOW, then sends SCLK and SDIN. When reading is complete and the interrupt mask data is in place, the controller de-asserts  $\overline{CS}$ . See [Figure 4](#) for register access timing.

### 7.1.1 $\overline{CS}$ - chip select

The  $\overline{CS}$  pin is the device chip select and is an active LOW input. The falling edge of  $\overline{CS}$  captures the input port status in the input status register. If the interrupt output is asserted, the falling edge of  $\overline{CS}$  will clear the interrupt. When  $\overline{CS}$  is LOW, the SPI interface is active. When  $\overline{CS}$  transitions HIGH the interrupt mask is stored and when  $\overline{CS}$  is HIGH, the SPI interface is disabled.

### 7.1.2 SCLK - serial clock input

SCLK is the serial clock input to the device. It should be LOW and remain LOW during the falling and rising edge of  $\overline{CS}$ . When  $\overline{CS}$  is LOW, the first rising edge of SCLK parallel loads the shift register from the input status register. The subsequent rising edges on SCLK serially shifts data out from the shift register. The falling edge of SCLK samples the data on SDIN.

### 7.1.3 SDIN - serial data input

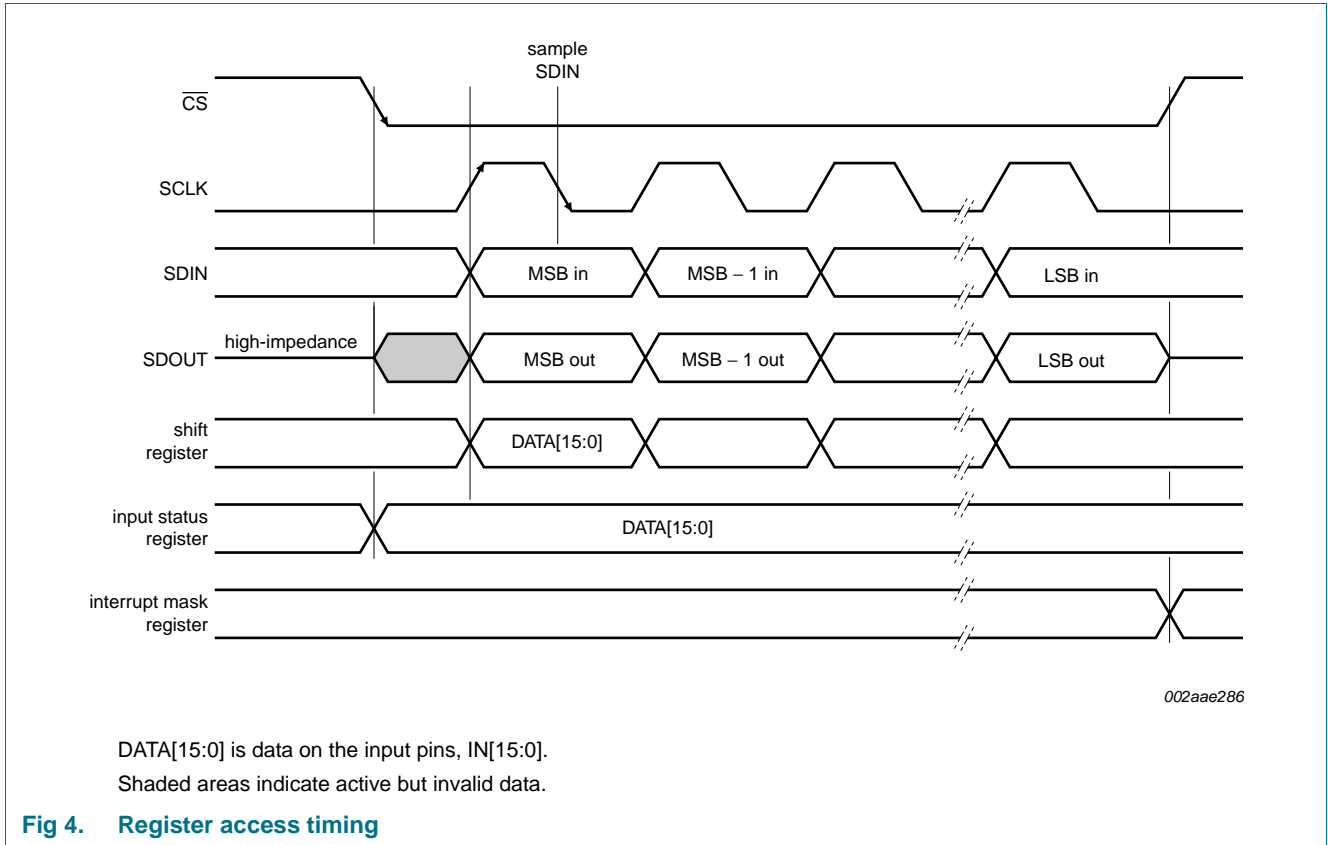
SDIN is the serial data input port. The data is sampled into the shift register on the falling edge of SCLK. SDIN is only active when  $\overline{CS}$  is LOW. This input has a 20  $\mu$ A pull-down current source to prevent the SDIN node from floating when  $\overline{CS}$  is HIGH.

### 7.1.4 SDO $\overline{U}$ T - serial data output

SDO $\overline{U}$ T is the serial data output signal. SDO $\overline{U}$ T is high-impedance when  $\overline{CS}$  is HIGH and switches to low-impedance after  $\overline{CS}$  goes LOW. When  $\overline{CS}$  is LOW, after the first rising edge of SCLK the most significant bit in the shift register is presented on SDO $\overline{U}$ T. Subsequent rising edges of SCLK shift the remaining data from the shift register onto SDO $\overline{U}$ T.

7.1.5 Register access timing

Figure 4 shows the waveforms of the device operation. Initially  $\overline{CS}$  is HIGH and SCLK is LOW. On the falling edge of  $\overline{CS}$ , input port status, DATA[n:0] is captured into the input status register, and subsequently the first rising edge of SCLK parallel loads the shift register. The falling edge of SCLK samples the data on the SDIN. The MSB from the shift register is valid and available on the SDOUT after the first rising edge of SCLK.



7.1.6 Software reset operation

Software reset will be activated by writing all zeroes into the shift register. This is identical to having an interrupt mask value of 0X00. Such an operation will reset the device, clear the input status register to zero and set the interrupt output to HIGH (no interrupt).

7.2 Interrupt output

$\overline{INT}$  is the open-drain interrupt output and is active LOW. A pull-up resistor of approximately 10 kΩ is recommended.

A user-defined interrupt mask bit pattern is shifted into the shift register via SDIN. The value of bits in the mask pattern will determine which input pins will cause an interrupt. Any bit that is = 0 will disable the input pin corresponding to that bit position from generating an interrupt. Interrupts will be enabled for bits having value = 1. The mask bit pattern is not automatically aligned with the desired input pins. It is the responsibility of the programmer to shift the correct number of (mask) bits to the correct positions into the shift

register. The interrupt mask bit pattern must be positioned into the shift register prior to the  $\overline{\text{CS}}$  rising edge. Misaligned mask pattern will result in unexpected activation of the interrupt signal.

The interrupt output is asserted when the input status is changed, and the interrupt mask bit corresponding to the input pin that caused the change is unmasked (bit value = 1), and is cleared on the falling edge of  $\overline{\text{CS}}$  or when the input port status matches the input status register. When there are multiple devices, the  $\overline{\text{INT}}$  outputs may be tied together to a single pull-up.

Table 3 illustrates the state of the interrupt output versus the state of the input port and input status register. The interrupt output is asserted when the input port and input status register differ.

**Table 3. Interrupt output function truth table**

H = HIGH; L = LOW; X = don't care

INT_EN	Input port status	Input status register <sup>[1]</sup>	$\overline{\text{INT}}$ output <sup>[2]</sup>	
			Mask bit = 1 (unmasked)	Mask bit = 0 (masked)
H	L	L	H	H
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H
L	X	X	H	H

[1] Input status register is the value or content of the D flip-flops.

[2] Logic states shown for  $\overline{\text{INT}}$  pin assumes 10 k $\Omega$  pull-up resistor.

### 7.3 Interrupt enable

INT\_EN is the interrupt output enable input and the general purpose input enable input. It is an active HIGH input. When the INT\_EN pin is LOW the GPI pins are turned off and the input state is saved to minimize power loss when the input pull-ups or pull-downs are cycled and the  $\overline{\text{INT}}$  output is disabled. The cycled pull-ups or pull-downs should be active sufficiently long before the INT\_EN is taken active that the GPI pin voltage is completely settled to prevent false or transient interrupt signals.

### 7.4 General Purpose Inputs

The General Purpose Inputs (GPI) are designed to behave like a typical input in the 0 V to 5.5 V range, but are also designed to have low leakage currents at elevated voltages. The input structure allows for elevated voltages to be applied through a series resistor. The series resistor is required when the input voltage is above 5.5 V. The series resistor is required for two reasons: first, to prevent damage to the input avalanche diode, and second, to prevent the ESD protection circuitry from creating an excessive current flow. The ESD protection circuitry includes a latch-back style device, which provides excellent ESD protection during assembly or typical 5.5 V applications. The series resistor limits the current flowing into the part and provides additional ESD protection. The limited current prevents the ESD latch-back device from latching back to a low voltage, which would cause excessive current flow and damage the part when the input voltage is above 5.5 V.



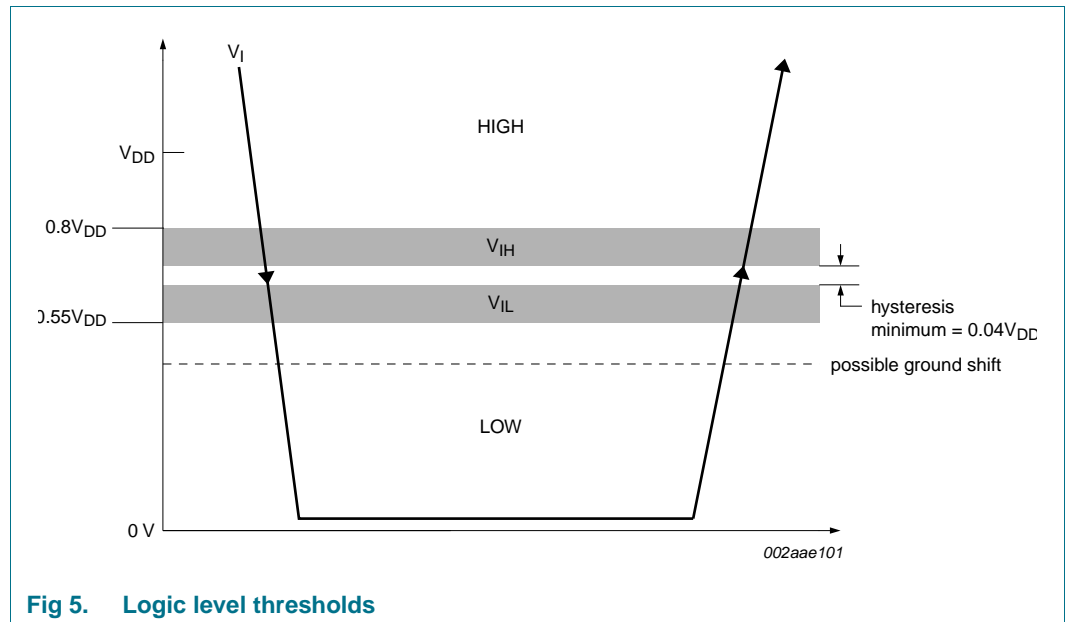
The minimum required series resistance for applications with input voltages above 5.5 V is 100 kΩ. For applications requiring an applied voltage above 27 V, [Equation 1](#) is recommended to determine the series resistor. Failure to include the appropriate input series resistor may result in product failure and will void the warranty.

$$R_s = \frac{\text{voltage applied} - 17 \text{ V}}{I_I} \tag{1}$$

The series resistor should be placed physically as close as possible to the connected input to reduce the effective node capacitance. The input response time is affected by the RC time constant of the series resistor and the input node capacitance.

**7.4.1 V<sub>IL</sub>, V<sub>IH</sub> and switching points**

A minimum LOW threshold of 2.5 V is guaranteed for the logical switching points for the inputs. See [Figure 5](#) for details.



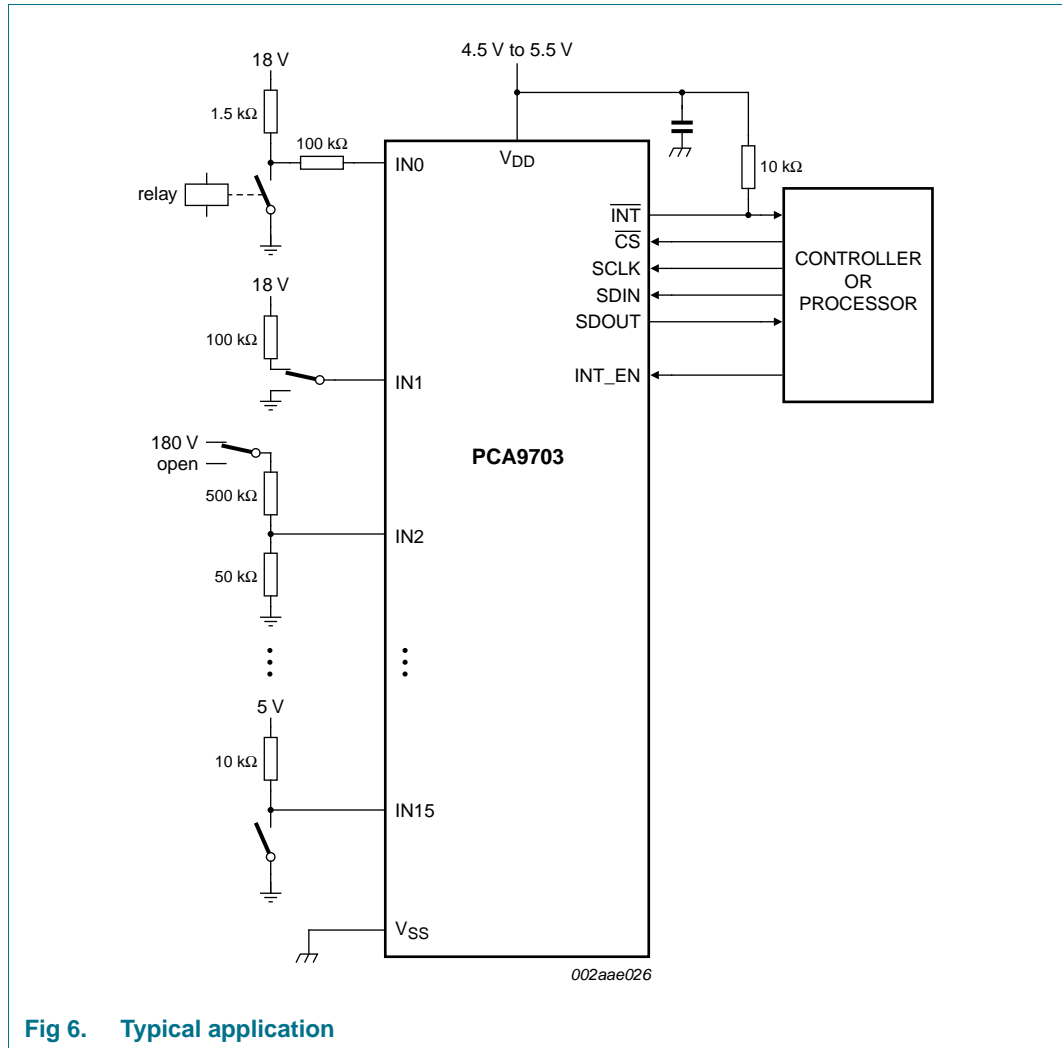
**Fig 5. Logic level thresholds**

The V<sub>IL</sub> is specified as a maximum of 0.55 × V<sub>DD</sub> and is 2.5 V at 4.5 V V<sub>DD</sub>. This means that if the user applies 2.5 V or less to the input (with V<sub>DD</sub> = 4.5 V), or as the voltage passes this threshold, they will always see a LOW.

The V<sub>IH</sub> is specified as a minimum of 0.8 × V<sub>DD</sub>. This means that if the user applies 3.6 V or more to the input (with V<sub>DD</sub> = 4.5 V), or as the voltage passes this threshold, they will always see a HIGH.

## 8. Application design-in information

### 8.1 General application



### 8.2 Automotive application

Supports:

- 12 V battery (8 V to 16 V)
- Double battery (16 V to 32 V)
- Reverse battery (−8 V to −16 V)
- Jump start (27 V for 60 seconds)
- Load dump (40 V)

**8.2.1 SBC wake port extension with cyclic biasing**

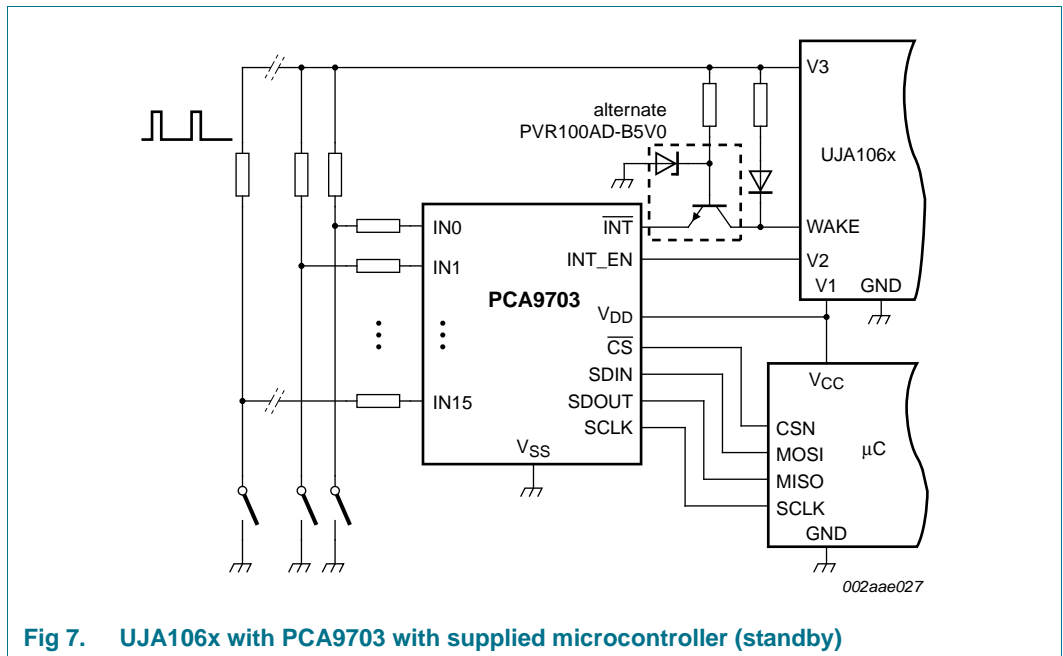
System Basis Chips (SBC) offer many functions needed for in-vehicle networking solutions. Some of the features built into SBC are:

- Transceivers (HS-CAN, LIN 2.0)
- Scalable voltage regulators
- Watchdog timers; wake-up function
- Fail-safe function

For more information on SBC, refer to

[www.nxp.com/products/interface\\_and\\_connectivity/system\\_basis\\_chips/](http://www.nxp.com/products/interface_and_connectivity/system_basis_chips/).

**8.2.1.1 UJA106x with PCA9703, standby**



**Fig 7. UJA106x with PCA9703 with supplied microcontroller (standby)**

- PCA9703 fits to SBC UJA106x and UJA107xA family
- PCA9703 can be powered by V1 of SBC
- Extends the SBC with 16 additional wake inputs
- µC can be set to stop-mode during standby to save ECU standby current. SBC with GPI periodically monitors the wake inputs
  - Cyclic bias via V3
  - Very low system current consumption even with clamped switches
  - Interrupt enable control via V2



8.2.2 Application examples including switches to battery

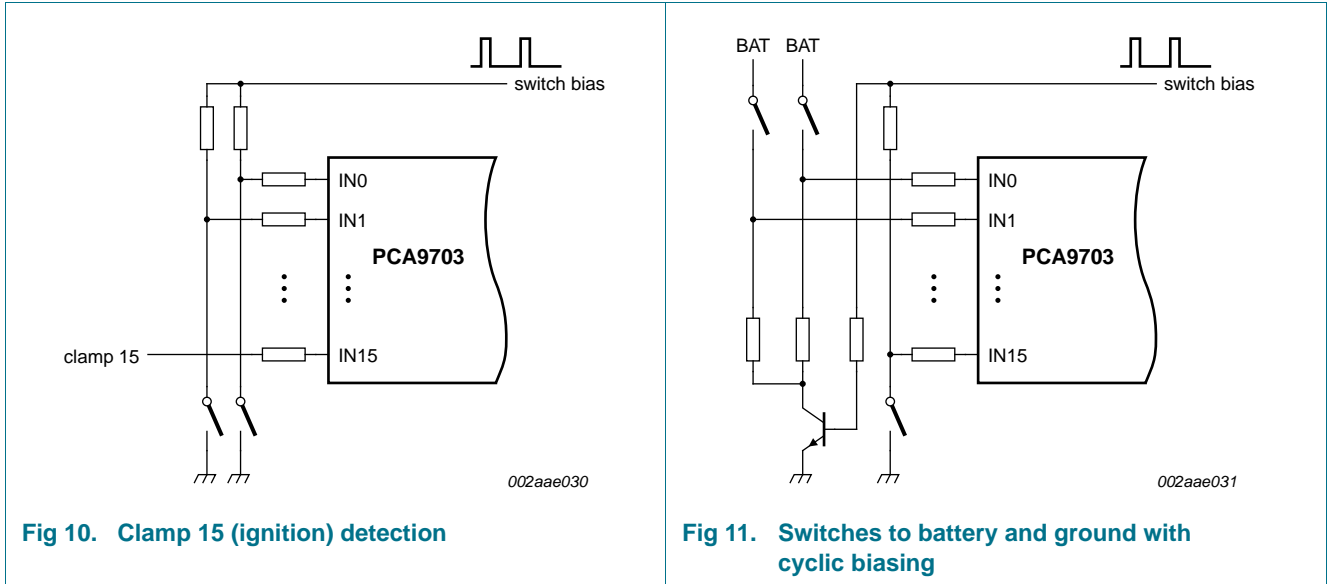


Fig 10. Clamp 15 (ignition) detection

Fig 11. Switches to battery and ground with cyclic biasing

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

T<sub>amb</sub> = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.0	V
I <sub>I</sub>	input current	IN[15:0] pins with series resistor and V <sub>I</sub> > 5.5 V	[1] -	350	µA
V <sub>I</sub>	input voltage	GPI pins IN[15:0]; no series resistor	[1] -0.5	+6	V
		SPI pins	-0.5	+6	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j(max)</sub>	maximum junction temperature	operating	-	125	°C

[1] With GPI external series resistors, the inputs support double battery, reverse battery and load dump conditions. During double battery or load dump the input pin will drain slightly higher leakage current until the input drops to 18 V. For more detail of leakage current specification, please refer to [Table 5 "Static characteristics"](#). See [Section 7.4](#) for series resistor requirements.

## 10. Static characteristics

**Table 5. Static characteristics**

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
$V_{DD}$	supply voltage		4.5	5.0	5.5	V
$I_{DD}$	supply current	$V_{DD} = 5.5\text{ V}$ ; input = 5 V or 18 V; $INT\_EN = V_{DD}$	-	1.0	2.5	$\mu\text{A}$
$V_{POR}$	power-on reset voltage		[1] -	1.8	2.2	V
<b>General Purpose Inputs (IN0 to IN15)</b>						
$V_{IL}$	LOW-level input voltage		[2] -	-	$0.55V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.8V_{DD}$	-	-	V
$V_{hys}$	hysteresis voltage	$V_{DD} = 4.5\text{ V}$	-	70	-	mV
$I_I$	input current	GPI recommended maximum current; $V_I > 5.5\text{ V}$ ; with series resistor $R_s$	[3] -	-	100	$\mu\text{A}$
$I_{IH}$	HIGH-level input current	each input; $V_I = V_{DD}$	-1	-	+1	$\mu\text{A}$
$I_{LI}$	input leakage current	$V_I = 17\text{ V}$ ; 100 k $\Omega$ series resistor	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$ or $V_{DD}$	-	2.0	5.0	pF
<b>Interrupt output (INT)</b>						
$I_{OL}$	LOW-level output current	$V_{DD} = 4.5\text{ V}$ ; $V_{OL} = 0.4\text{ V}$	6	-	-	mA
$I_{OH}$	HIGH-level output current	$V_{OH} = V_{DD}$	-1	-	+1	$\mu\text{A}$
$C_o$	output capacitance		-	2	5	pF
<b>SPI and control (SDOUT, SDIN, SCLK, <math>\overline{CS}</math>, INT_EN)</b>						
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
$I_{IH}$	HIGH-level input current	SDIN; $V_I = V_{DD} = 5.5\text{ V}$	-	20	40	$\mu\text{A}$
$I_{OL}$	LOW-level output current	SDOUT; $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 4.5\text{ V}$	5	-	-	mA
$I_{OH}$	HIGH-level output current	SDOUT; $V_{OH} = V_{DD} - 0.5\text{ V}$ ; $V_{DD} = 4.5\text{ V}$	-5	-11	-	mA
$C_i$	input capacitance	$V_I = V_{SS}$ or $V_{DD}$	-	2	5	pF
$C_o$	output capacitance	SDOUT; $\overline{CS} = V_{DD}$	-	4	6	pF

[1]  $V_{DD}$  must be lowered to 0.2 V for at least 5  $\mu\text{s}$  in order to reset device.

[2] Minimum  $V_{IL}$  is 2.5 V at  $V_{DD} = 4.5\text{ V}$ .

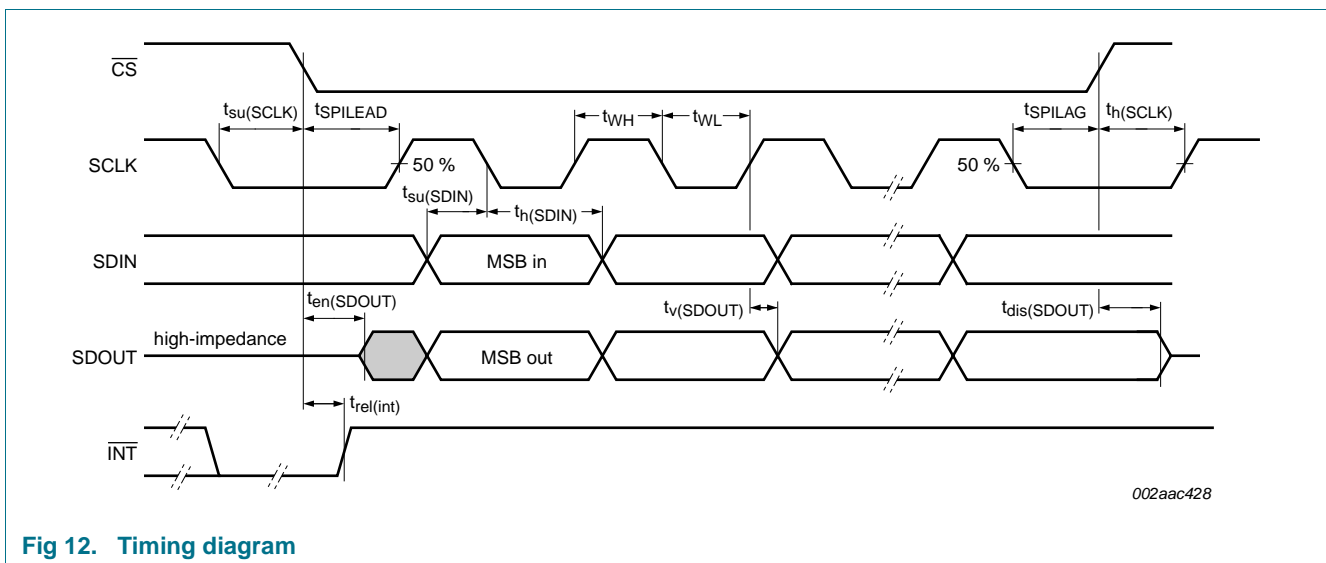
[3] For GPI pin voltages > 5.5 V, see [Section 7.4](#).

## 11. Dynamic characteristics

**Table 6. Dynamic characteristics**

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{max}$	maximum input clock frequency		-	-	5	MHz
$t_r$	rise time	SDOUT; 10 % to 90 % at 5 V	-	35	60	ns
$t_f$	fall time	SDOUT; 90 % to 10 % at 5 V	-	25	50	ns
$t_{WH}$	pulse width HIGH	SCLK	50	-	-	ns
$t_{WL}$	pulse width LOW	SCLK	50	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	$\overline{CS}$ falling edge to SCLK rising edge	50	-	-	ns
$t_{SPILAG}$	SPI enable lag time	SCLK falling edge to $\overline{CS}$ rising edge	50	-	-	ns
$t_{su(SDIN)}$	SDIN set-up time	SDIN to SCLK falling edge	20	-	-	ns
$t_{h(SDIN)}$	SDIN hold time	from SCLK falling edge	30	-	-	ns
$t_{en(SDOUT)}$	SDOUT enable time	from $\overline{CS}$ LOW to SDOUT low-impedance; <a href="#">Figure 15</a>	-	-	55	ns
$t_{dis(SDOUT)}$	SDOUT disable time	from rising edge of $\overline{CS}$ to SDOUT high-impedance; <a href="#">Figure 15</a>	-	-	85	ns
$t_v(SDOUT)$	SDOUT valid time	from rising edge of SCLK; <a href="#">Figure 16</a>	-	-	55	ns
$t_{su(SCLK)}$	SCLK set-up time	SCLK falling to $\overline{CS}$ falling	50	-	-	ns
$t_{h(SCLK)}$	SCLK hold time	SCLK rising after $\overline{CS}$ rising	50	-	-	ns
$t_{POR}$	power-on reset pulse time	time before $\overline{CS}$ is active after $V_{DD} > V_{POR}$	-	-	250	ns
$t_{rel(int)}$	interrupt release time	after $\overline{CS}$ going LOW; <a href="#">Figure 17</a>	-	-	500	ns
$t_v(INT)$	valid time on pin $\overline{INT}$	after $IN_n$ changes or $INT\_EN$ goes HIGH	-	200	800	ns



**Fig 12. Timing diagram**

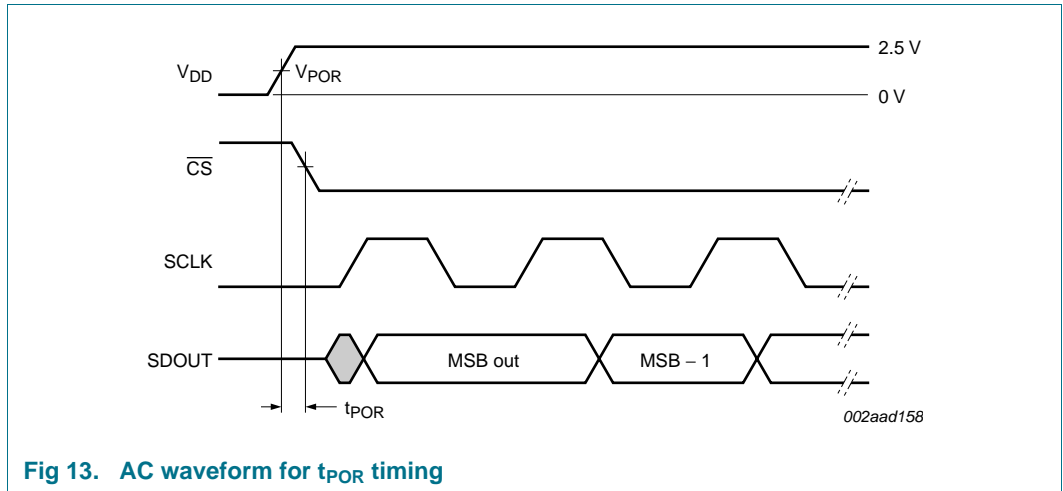


Fig 13. AC waveform for  $t_{POR}$  timing

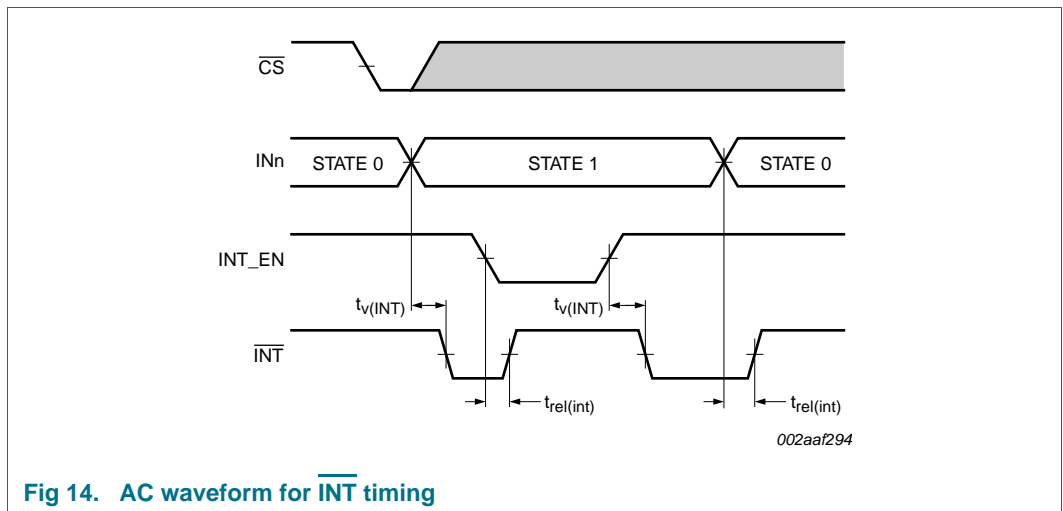


Fig 14. AC waveform for  $\overline{INT}$  timing



12. Test information

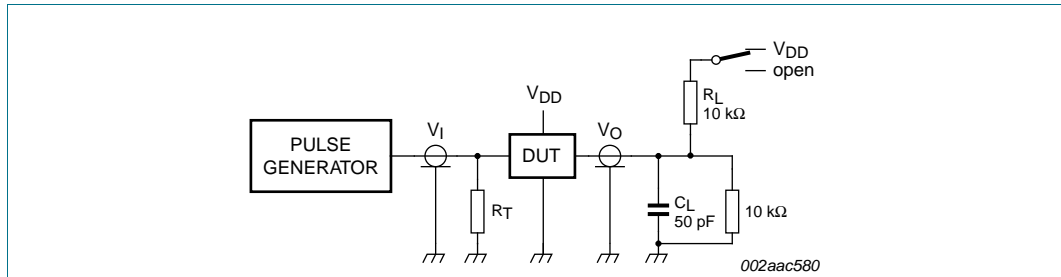


Fig 15. Test circuitry for enable/disable times, SDOUT ( $t_{\text{en}}(\text{SDOUT})$  and  $t_{\text{dis}}(\text{SDOUT})$ )

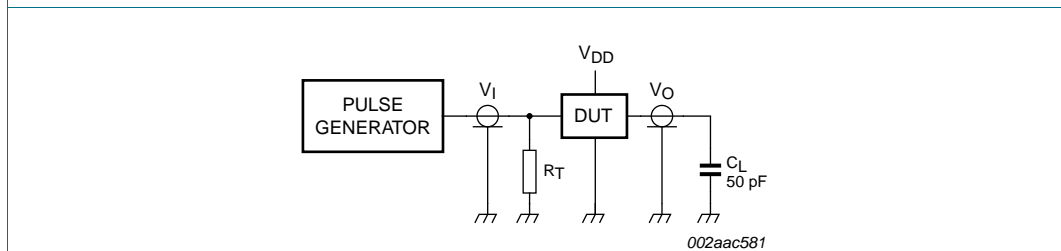


Fig 16. Test circuitry for switching times, SDOUT ( $t_v(\text{SDOUT})$ )

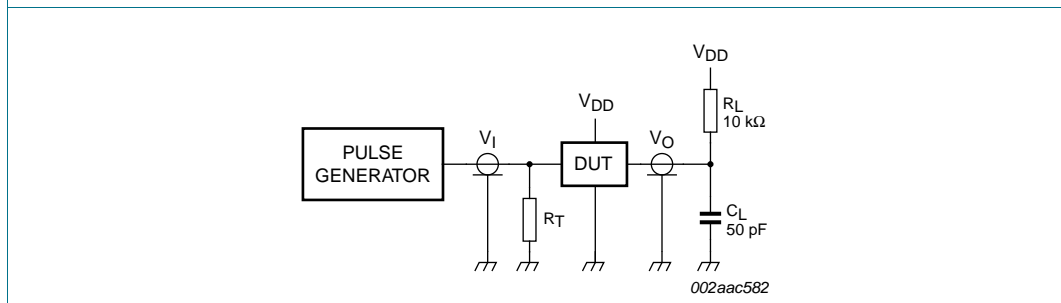


Fig 17. Test circuitry for switching times,  $\overline{\text{INT}}$

$R_L$  = load resistance.

$C_L$  = load capacitance includes jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generators.

13. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

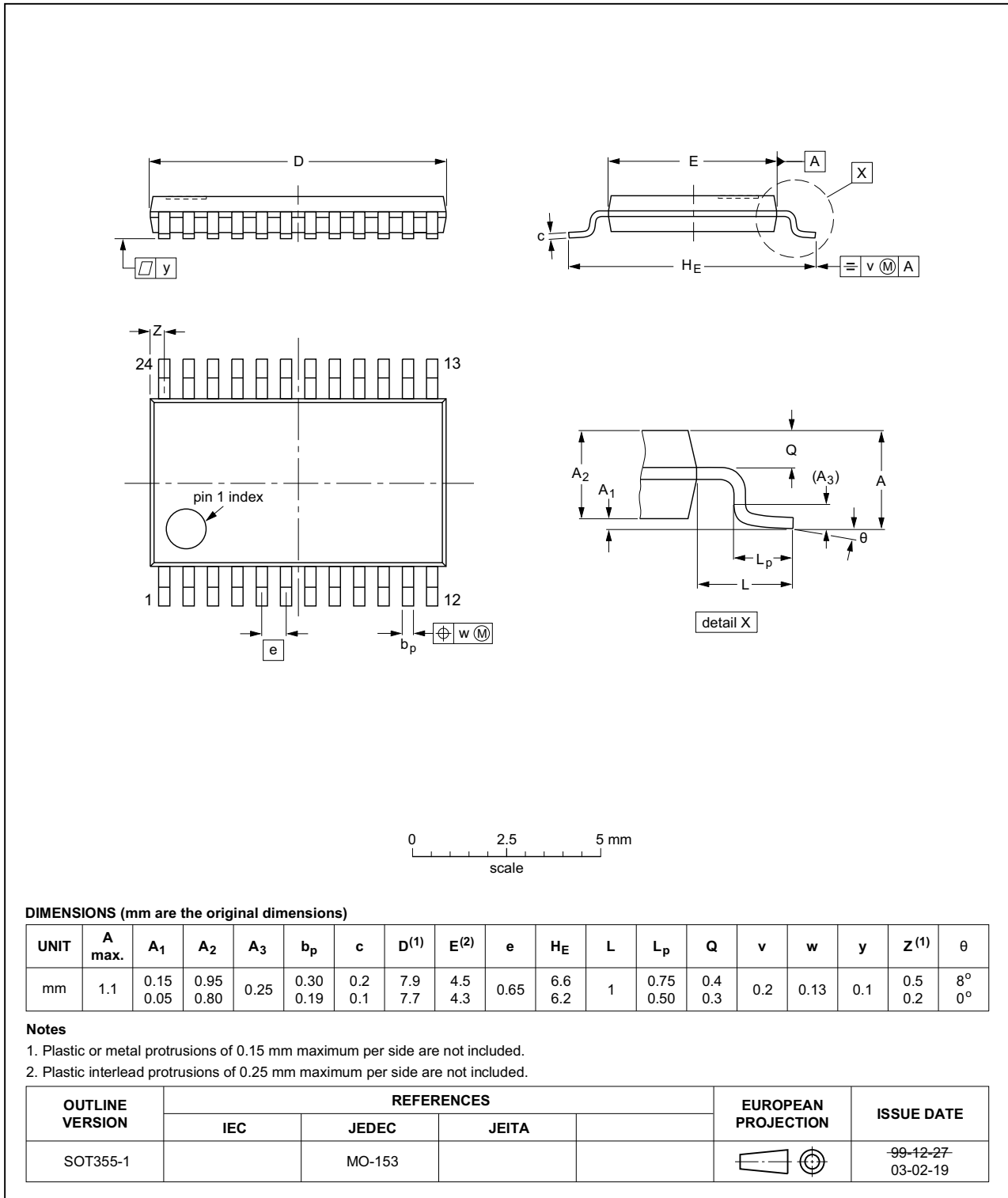


Fig 18. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.75 mm

SOT994-1

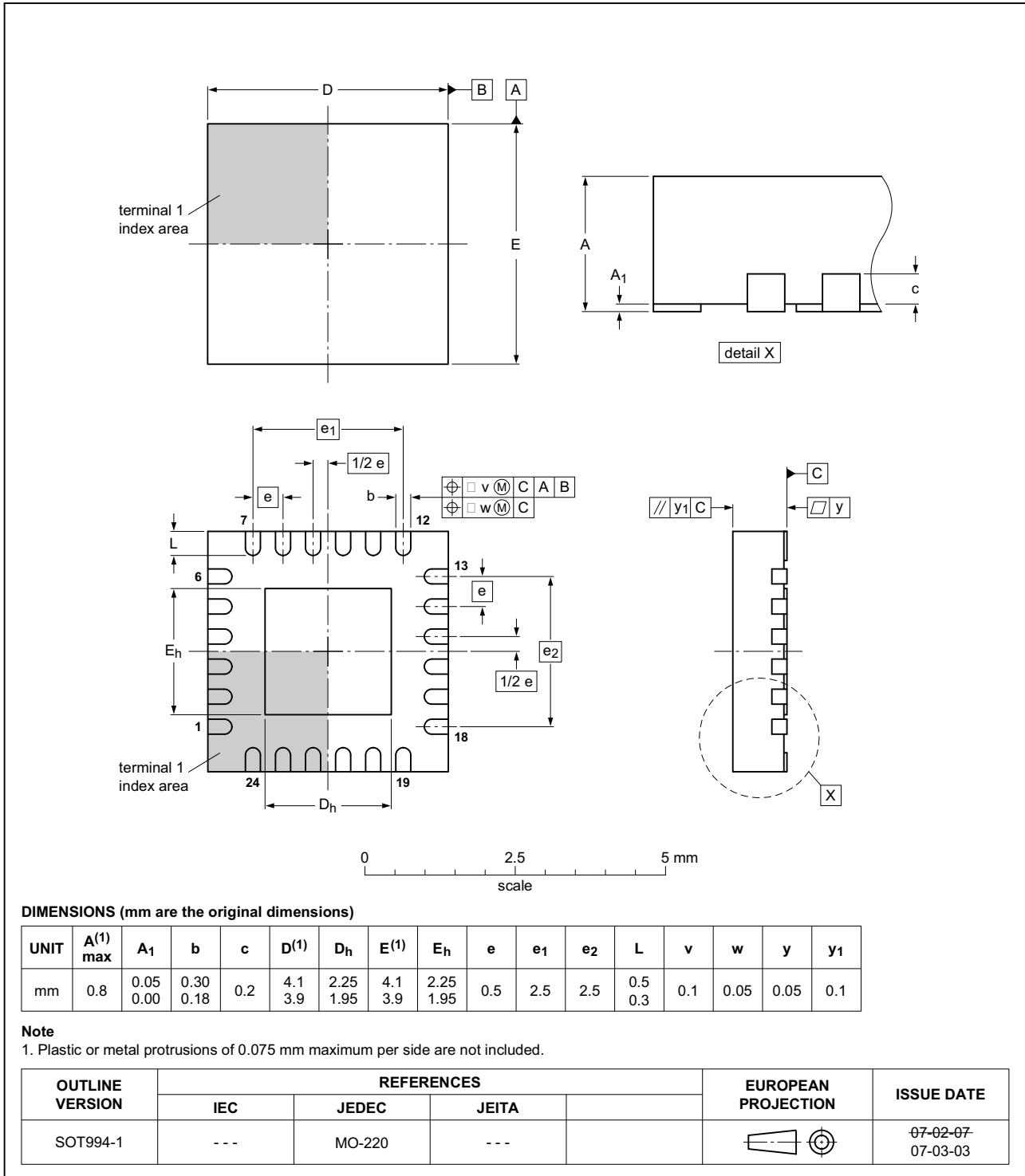


Fig 19. Package outline SOT994-1 (HWQFN24)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#) and [8](#)

**Table 7. SnPb eutectic process (from J-STD-020D)**

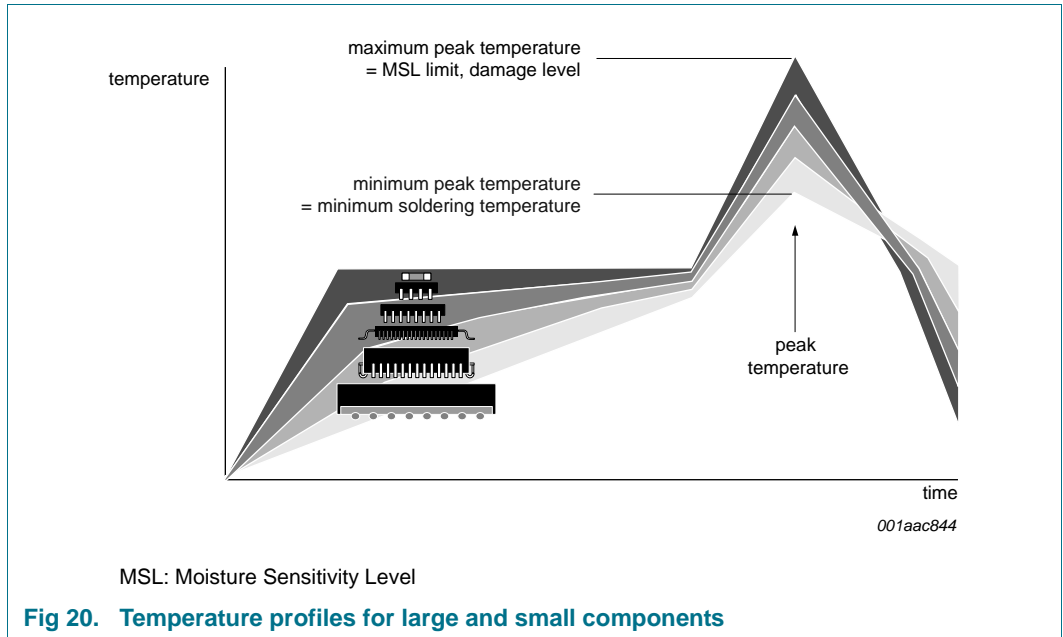
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 8. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).

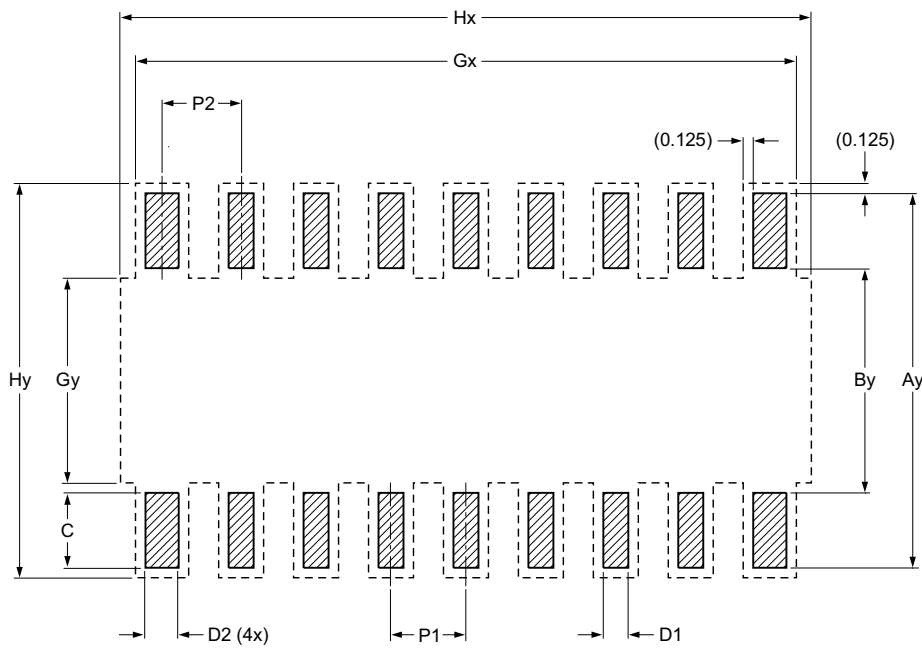


For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.


15. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP24 package

SOT355-1



Generic footprint pattern  
Refer to the package outline drawing for actual layout

 solder land

----- occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1\_fr

Fig 21. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

Footprint information for reflow soldering of HVQFN24 package

SOT994-1

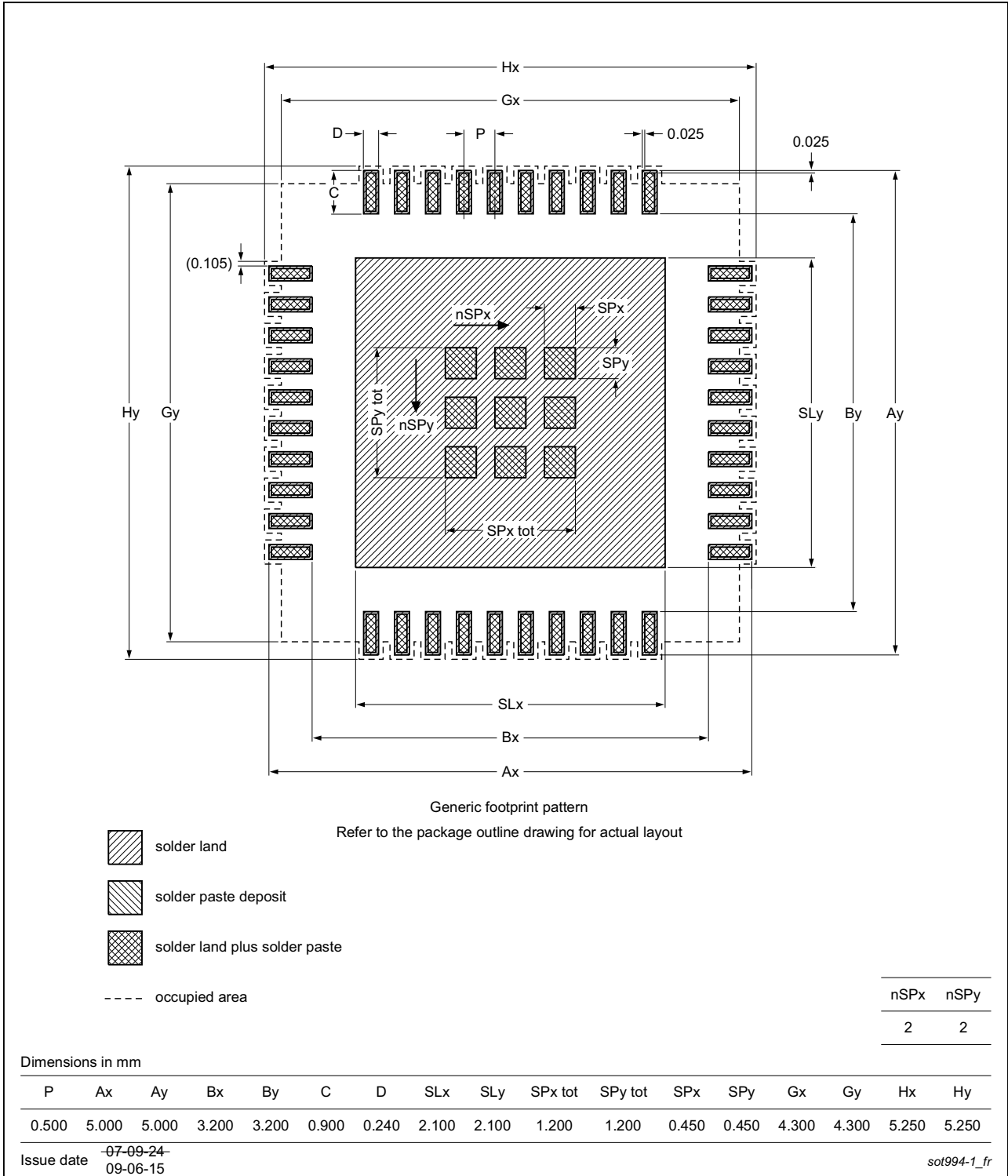


Fig 22. PCB footprint for SOT994-1 (HVQFN24); reflow soldering



## 16. Abbreviations

Table 9. Abbreviations

Acronym	Description
ASSP	Application Specific Standard Product
CAN	Controller Area Network
CDM	Charged-Device Model
DUT	Device Under Test
ECU	Electronic Control Unit
ESD	ElectroStatic Discharge
GPI	General Purpose Input
HBM	Human Body Model
HS-CAN	High-Speed Controller Area Network
LIN	Local Interconnect Network
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PPAP	Production Part Approval Process
RC	Resistor-Capacitor network
SBC	System Basis Chip
SPI	Serial Peripheral Interface
μC	microcontroller

## 17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9703 v.4	20140905	Product data sheet	-	PCA9703 v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 5</a>, <math>V_{hys}</math>: Updated conditions, min, typ and unit. Removed table note [3]. Aligned to characterization data, no change to device.</li> <li>• Removed references to hysteresis in <a href="#">Section 2</a>, <a href="#">Figure 5</a>, <a href="#">Section 7.4.1</a>.</li> </ul>			
PCA9703 v.3	20140317	Product data sheet	-	PCA9703 v.2
PCA9703 v.2	20120614	Product data sheet	-	PCA9703 v.1
PCA9703 v.1	20100223	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 20. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>18.3</b>	Disclaimers . . . . .	<b>26</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	<b>18.4</b>	Trademarks . . . . .	<b>27</b>
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>	<b>19</b>	<b>Contact information</b> . . . . .	<b>27</b>
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>	<b>20</b>	<b>Contents</b> . . . . .	<b>28</b>
<b>5</b>	<b>Block diagram</b> . . . . .	<b>3</b>			
<b>6</b>	<b>Pinning information</b> . . . . .	<b>3</b>			
6.1	Pinning . . . . .	3			
6.2	Pin description . . . . .	4			
<b>7</b>	<b>Functional description</b> . . . . .	<b>5</b>			
7.1	SPI bus operation . . . . .	6			
7.1.1	CS - chip select . . . . .	6			
7.1.2	SCLK - serial clock input . . . . .	6			
7.1.3	SDIN - serial data input . . . . .	6			
7.1.4	SDOUT - serial data output . . . . .	6			
7.1.5	Register access timing . . . . .	7			
7.1.6	Software reset operation . . . . .	7			
7.2	Interrupt output . . . . .	7			
7.3	Interrupt enable . . . . .	8			
7.4	General Purpose Inputs . . . . .	8			
7.4.1	V <sub>IL</sub> , V <sub>IH</sub> and switching points . . . . .	9			
<b>8</b>	<b>Application design-in information</b> . . . . .	<b>10</b>			
8.1	General application . . . . .	10			
8.2	Automotive application . . . . .	10			
8.2.1	SBC wake port extension with cyclic biasing . . . . .	11			
8.2.1.1	UJA106x with PCA9703, standby . . . . .	11			
8.2.1.2	UJA107xA with PCA9703, standby and sleep . . . . .	12			
8.2.2	Application examples including switches to battery . . . . .	13			
<b>9</b>	<b>Limiting values</b> . . . . .	<b>13</b>			
<b>10</b>	<b>Static characteristics</b> . . . . .	<b>14</b>			
<b>11</b>	<b>Dynamic characteristics</b> . . . . .	<b>15</b>			
<b>12</b>	<b>Test information</b> . . . . .	<b>17</b>			
<b>13</b>	<b>Package outline</b> . . . . .	<b>18</b>			
<b>14</b>	<b>Soldering of SMD packages</b> . . . . .	<b>20</b>			
14.1	Introduction to soldering . . . . .	20			
14.2	Wave and reflow soldering . . . . .	20			
14.3	Wave soldering . . . . .	20			
14.4	Reflow soldering . . . . .	21			
<b>15</b>	<b>Soldering: PCB footprints</b> . . . . .	<b>23</b>			
<b>16</b>	<b>Abbreviations</b> . . . . .	<b>25</b>			
<b>17</b>	<b>Revision history</b> . . . . .	<b>25</b>			
<b>18</b>	<b>Legal information</b> . . . . .	<b>26</b>			
18.1	Data sheet status . . . . .	26			
18.2	Definitions . . . . .	26			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2014.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 5 September 2014

Document identifier: PCA9703