

## LP3853/LP3856 3A Fast Response Ultra Low Dropout Linear Regulators

Check for Samples: LP3853, LP3856

#### **FEATURES**

- Ultra Low Dropout Voltage
- Stable with Selected Ceramic Capacitors
- Low Ground Pin Current
- Load Regulation of 0.08%
- 10nA Quiescent Current in Shutdown Mode
- Ensured Output Current of 3A DC
- Available in TO-263 and TO-220 Packages
- Output Voltage Accuracy ± 1.5%
- Error Flag Indicates Output Status
- Sense Option Improves Load Regulation
- Overtemperature/overcurrent Protection
- -40°C to +125°C Junction Temperature Range

#### **APPLICATIONS**

- Microprocessor Power Supplies
- Stable with Ceramic Output Capacitors
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- High Efficiency Linear Regulators
- Battery Chargers
- Other Battery Powered Applications

#### DESCRIPTION

The LP3853/LP3856 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3853/LP3856 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3853/LP3856 to operate under extremely low dropout conditions.

**Dropout Voltage:** Ultra low dropout voltage; typically 39mV at 300mA load current and 390mV at 3A load current.

**Ground Pin Current:** Typically 4mA at 3A load current.

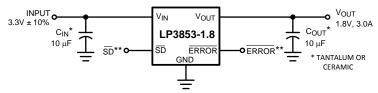
**Shutdown Mode:** Typically 10nA quiescent current when the shutdown pin is pulled low.

**Error** Flag: Error flag goes low when the output voltage drops 10% below nominal value.

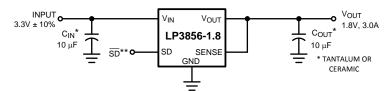
**SENSE:** Sense pin improves regulation at remote loads.

**Precision Output Voltage:** Multiple output voltage options are available ranging from 1.8V to 5.0V with a ensured accuracy of  $\pm 1.5\%$  at room temperature, and  $\pm 3.0\%$  over all conditions (varying line, load, and temperature).

## **Typical Application Circuits**



\*\*SD and ERROR pins must be pulled high through a 10kΩ pull-up resistor. Connect the ERROR pin to ground if this function is not used. See Application Hints for more information.



\*\*\$D pin must be pulled high through a 10kΩ pull-up resistor. See Application Hints for more information.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



## **Connection Diagram**

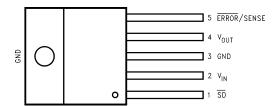


Figure 1. Top View TO220-5 Package Bent, Staggered Leads

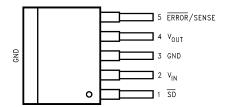


Figure 2. Top View TO263-5 Package

Table 1. Pin Description for TO220-5 and TO263-5 Packages

Pin #		LP3853		LP3856
Pin #	Name	Function	Name	Function
1	SD	Shutdown	SD	Shutdown
2	V <sub>IN</sub>	Input Supply	V <sub>IN</sub>	Input Supply
3	GND	Ground	GND	Ground
4	V <sub>OUT</sub>	Output Voltage	V <sub>OUT</sub>	Output Voltage
5	ERROR	ERROR Flag	SENSE	Remote Sense Pin

## **Block Diagram**

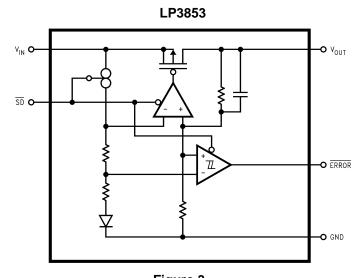


Figure 3.



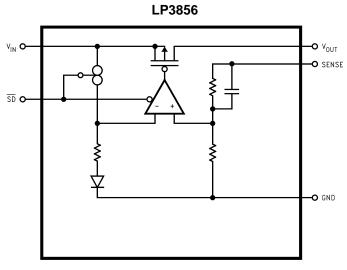


Figure 4.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)

Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 5 sec.)	260°C
ESD Rating (2)	2 kV
Power Dissipation (3)	Internally Limited
Input Supply Voltage (Survival)	-0.3V to +7.5V
Shutdown Input Voltage (Survival)	-0.3V to 7.5V
Output Voltage (Survival), (4), (5)	-0.3V to +6.0V
I <sub>OUT</sub> (Survival)	Short Circuit Protected
Maximum Voltage for ERROR Pin	V <sub>IN</sub>
Maximum Voltage for SENSE Pin	V <sub>OUT</sub>

- (1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.
- (3) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at  $\theta_{jA} = 50^{\circ}$ C/W (with 0.5in<sup>2</sup>, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at  $\theta_{jA} = 60^{\circ}$ C/W (with 0.5in<sup>2</sup>, 1oz. copper area), junction-to-ambient. See Application Hints. If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
- The output PMOS structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

## **Operating Ratings**

Input Supply Voltage (1)	2.5V to 7.0V
Shutdown Input Voltage	-0.3V to 7.0V
Maximum Operating Current (DC)	3A
Junction Temperature	−40°C to +125°C

(1) The minimum operating value for V<sub>IN</sub> is equal to either [V<sub>OUT(NOM)</sub> + V<sub>DROPOUT</sub>] or 2.5V, whichever is greater.



## Electrical Characteristics LP3853/LP3856

Limits in standard typeface are for  $T_J = 25^{\circ}C$ , and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified:  $V_{IN} = V_{O(NOM)} + 1V$ ,  $I_L = 10$  mA,  $C_{OUT} = 10\mu F$ ,  $V_{SD} = 2V$ .

		0 1111	- (1)	LP385	l lmite		
Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Min	Max	Units	
Vo	Output Voltage Tolerance	$V_{OUT} + 1V \le V_{IN} \le 7.0V$ 10 mA $\le I_L \le 3A$	0	-1.5 <b>-3.0</b>	+1.5 +3.0	%	
$\Delta$ V $_{OL}$	Output Voltage Line Regulation	$V_{OUT} + 1V \le V_{IN} \le 7.0V$	0.02 <b>0.06</b>			%	
$\Delta V_{O}/\Delta I_{OUT}$	Output Voltage Load Regulation	10 mA ≤ I <sub>L</sub> ≤ 3A	0.08 <b>0.14</b>			%	
., .,	Dropout Voltage	I <sub>L</sub> = 300 mA	39		50 <b>65</b>	>/	
V <sub>IN</sub> - V <sub>OUT</sub>	(4)	I <sub>L</sub> = 3A	390		450 <b>600</b>	mV	
	Ground Pin Current In Normal	I <sub>L</sub> = 300 mA	4		9 <b>10</b>	A	
$I_{GND}$	Operation Mode	I <sub>L</sub> = 3A	4		9 <b>10</b>	mA	
	Ground Pin Current In Shutdown	V <sub>SD</sub> ≤ 0.3V	0.01		10	μA	
$I_{GND}$	Mode	-40°C ≤ T <sub>J</sub> ≤ 85°C			50		
I <sub>O(PK)</sub>	Peak Output Current	V <sub>O</sub> ≥ V <sub>O(NOM)</sub> - 4%	4.5			Α	
hort Circuit I	Protection						
I <sub>SC</sub>	Short Circuit Current		6			Α	
hutdown Inp	ut	,			•	*	
.,	Object description of the control of	V <sub>SDT</sub> Rising from 0.3V until Output = ON	1.3	2			
$V_{SDT}$	Shutdown Threshold	V <sub>SDT</sub> Falling from 2.0V until Output = OFF	1.3		0.3	V	
T <sub>dOFF</sub>	Turn-off delay	I <sub>L</sub> = 3A	20			μs	
$T_{dON}$	Turn-on delay	I <sub>L</sub> = 3A	25			μs	
I <sub>SD</sub>	SD Input Current	$V_{SD} = V_{IN}$	1			nA	
rror Flag							
$V_{T}$	Threshold	(5)	10	5	16	%	
$V_{TH}$	Threshold Hysteresis	(5)	5	2	8	%	
V <sub>EF(Sat)</sub>	Error Flag Saturation	$I_{sink} = 100\mu A$	0.02		0.1	V	
Td	Flag Reset Delay		1			μs	
I <sub>lk</sub>	Error Flag Pin Leakage Current		1			nA	
I <sub>max</sub>	Error Flag Pin Sink Current	V <sub>Error</sub> = <b>0.5V</b>	1			mA	

<sup>(1)</sup> Typical numbers are at 25°C and represent the most likely parametric norm.

<sup>(2)</sup> Limits are ensured by testing, design, or statistical correlation.

<sup>(3)</sup> Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

<sup>(4)</sup> Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

<sup>(5)</sup> Error Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.



# Electrical Characteristics LP3853/LP3856 (continued)

Limits in standard typeface are for  $T_J = 25^{\circ}C$ , and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified:  $V_{IN} = V_{O(NOM)} + 1V$ ,  $I_L = 10$  mA,  $C_{OUT} = 10\mu F$ ,  $V_{SD} = 2V$ .

0	D	O and Millians	T (1)	LP385			
Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Min	Max	Units	
AC Parameter	'S						
PSRR	Dinale Dejection	$V_{IN} = V_{OUT} + 1V$ $C_{OUT} = 10 uF$ $V_{OUT} = 3.3V, f = 120 Hz$	73			- dB	
PSKK	Ripple Rejection	V <sub>IN</sub> = V <sub>OUT</sub> + 0.5V C <sub>OUT</sub> = 10uF V <sub>OUT</sub> = 3.3V, f = 120Hz				uВ	
ρ <sub>n(I/f</sub>	Output Noise Density	f = 120Hz	0.8			μV	
	Output Naige Voltage	$BW = 10Hz - 100kHz$ $V_{OUT} = 2.5V$	150			\/ (=====)	
e <sub>n</sub>	Output Noise Voltage	BW = 300Hz - 300kHz $V_{OUT} = 2.5V$	100			μV (rms)	



## **Typical Performance Characteristics**

Unless otherwise specified:  $T_J$  = 25°C,  $C_{OUT}$  = 10 $\mu$ F,  $C_{IN}$  = 10 $\mu$ F, S/D pin is tied to  $V_{IN}$ ,  $V_{OUT}$  = 2.5V,  $V_{IN}$  =  $V_{O(NOM)}$  + 1V,  $I_L$  = 10 mA.

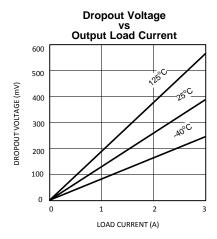


Figure 5.

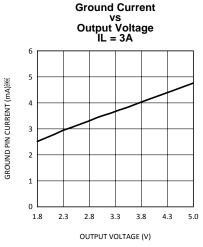


Figure 7.

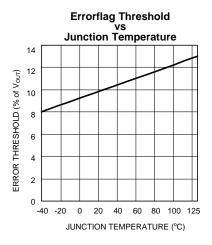
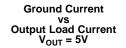


Figure 9.



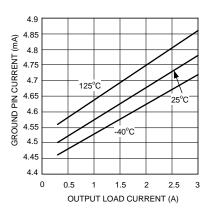


Figure 6.

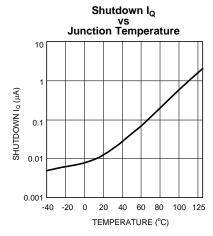


Figure 8.

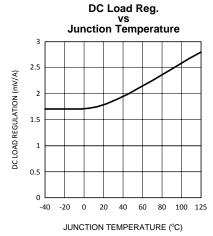


Figure 10.



## **Typical Performance Characteristics (continued)**

Unless otherwise specified:  $T_J = 25^{\circ}C$ ,  $C_{OUT} = 10 \mu F$ ,  $C_{IN} = 10 \mu F$ , S/D pin is tied to  $V_{IN}$ ,  $V_{OUT} = 2.5 V$ ,

 $V_{IN} = V_{O(NOM)} + 1V$ ,  $I_L = 10$  mA.

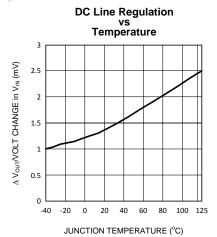


Figure 11.

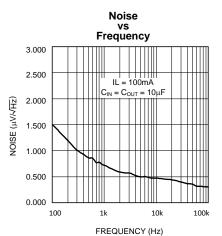


Figure 13.

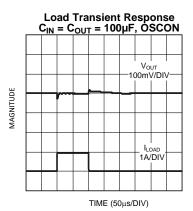


Figure 15.

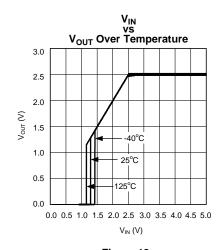


Figure 12.

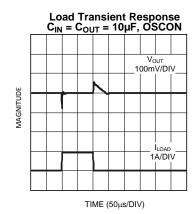
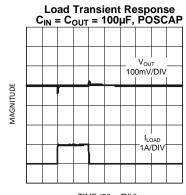


Figure 14.

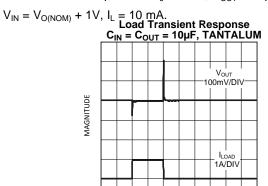


TIME (50μs/DIV) Figure 16.



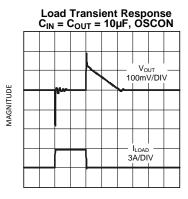
## **Typical Performance Characteristics (continued)**

Unless otherwise specified:  $T_J$  = 25°C,  $C_{OUT}$  = 10 $\mu$ F,  $C_{IN}$  = 10 $\mu$ F, S/D pin is tied to  $V_{IN}$ ,  $V_{OUT}$  = 2.5V,



TIME (50 $\mu$ s/DIV)

Figure 17.



TIME (50μs/DIV) **Figure 19.** 

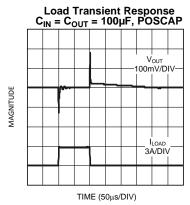


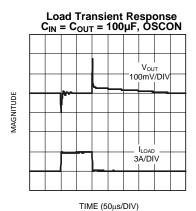
Figure 21.

Load Transient Response  $C_{IN} = C_{OUT} = 100 \mu F$ , TANTALUM

Vout
100mV/DIV
1A/DIV

TIME (50µs/DIV)

Figure 18.



IIVIE (50μS/DIV)

Figure 20.

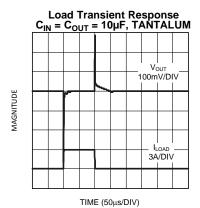
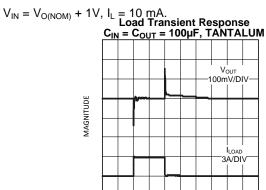


Figure 22.



## **Typical Performance Characteristics (continued)**

Unless otherwise specified:  $T_J = 25$ °C,  $C_{OUT} = 10 \mu F$ ,  $C_{IN} = 10 \mu F$ , S/D pin is tied to  $V_{IN}$ ,  $V_{OUT} = 2.5 V$ ,



TIME (50μs/DIV) Figure 23.

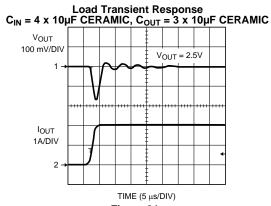
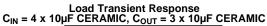


Figure 24.



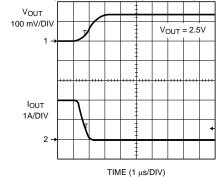
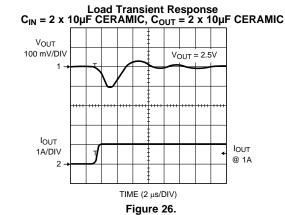


Figure 25.



# Load Transient Response $C_{IN} = 2 \times 10 \mu F$ CERAMIC, $C_{OUT} = 2 \times 10 \mu F$ CERAMIC

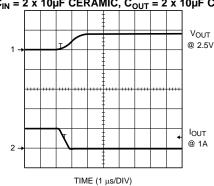


Figure 27.

Copyright © 2003–2013, Texas Instruments Incorporated



#### APPLICATION INFORMATION

### **Application Hints**

#### **EXTERNAL CAPACITORS**

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

**INPUT CAPACITOR:** An input capacitor of at least 10µF is required. Ceramic or Tantalum may be used, and capacitance may be increased without limit

**OUTPUT CAPACITOR:** An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum amount of output capacitance that can be used for stable operation is  $10\mu\text{F}$ . For general usage across all load currents and operating conditions, the part was characterized using a  $10\mu\text{F}$  Tantalum input capacitor. The minimum and maximum stable ESR range for the output capacitor was then measured which kept the device stable, assuming any output capacitor whose value is greater than  $10\mu\text{F}$  (see Figure 28 below).

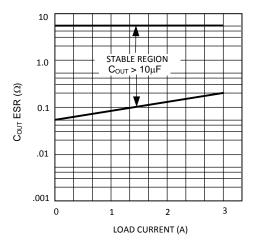


Figure 28. ESR Curve for C<sub>OUT</sub> (with 10µF Tantalum Input Capacitor)

It should be noted that it is possible to operate the part with an output capacitor whose ESR is below these limits, assuming that sufficient ceramic input capacitance is provided. This will allow stable operation using ceramic output capacitors (see next section).

#### **OPERATION WITH CERAMIC OUTPUT CAPACITORS**

LP385X voltage regulators can operate with ceramic output capacitors if the values of input and output capacitors are selected appropriately. The total ceramic output capacitance must be equal to or less than a specified maximum value in order for the regulator to remain stable over all operating conditions. This maximum amount of ceramic output capacitance is dependent upon the amount of ceramic input capacitance used as well as the load current of the application. This relationship is shown in Figure 29, which graphs the maximum stable value of ceramic output capacitance as a function of ceramic input capacitance for load currents of 1A, 2A, and 3A. For example, if the maximum load current is 1A, a  $10\mu F$  ceramic input capacitor will allow stable operation for values of ceramic output capacitance from  $10\mu F$  up to about  $500\mu F$ .



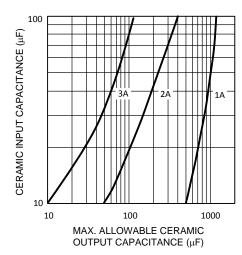


Figure 29. Maximum Ceramic Output Capacitance vs Ceramic Input Capacitance

If the maximum load current is 2A and a  $10\mu F$  ceramic input capacitor is used, the regulator will be stable with ceramic output capacitor values from  $10\mu F$  up to about  $50\mu F$ . At 3A of load current, the ratio of input to output capacitance required approaches 1:1, meaning that whatever amount of ceramic output capacitance is used must also be provided at the input for stable operation. For load currents between 1A, 2A, and 3A, interpolation may be used to approximate values on the graph. When calculating the total ceramic output capacitance present in an application, it is necessary to include any ceramic bypass capacitors connected to the regulator output.

#### **SELECTING A CAPACITOR**

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see Capacitor Characteristics Section).

#### **CAPACITOR CHARACTERISTICS**

**CERAMIC:** For values of capacitance in the 10 to 100  $\mu$ F range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 m $\Omega$ ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

**TANTALUM:** Solid Tantalum capacitors are typically recommended for use on the output because their ESR is very close to the ideal value required for loop compensation.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.



The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

**ALUMINUM:** This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to -40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP385X. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

#### TURN-ON CHARACTERISTICS FOR OUTPUT VOLTAGES PROGRAMMED TO 2.0V OR BELOW

As Vin increases during start-up, the regulator output will track the input until Vin reaches the minimum operating voltage (typically about 2.2V). For output voltages programmed to 2.0V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2.0V are not affected by this behavior.

#### **PCB LAYOUT**

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out  $C_{IN}$  and  $C_{OUT}$  near the device with short traces to the  $V_{IN}$ ,  $V_{OUT}$ , and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem.

Since high current flows through the traces going into  $V_{IN}$  and coming from  $V_{OUT}$ , Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

#### RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

www.ti.com

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

#### **OUTPUT NOISE**

Noise is specified in two ways-

**Spot Noise** or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

**Total output Noise** or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units  $\mu V/\sqrt{Hz}$  or  $nV/\sqrt{Hz}$  and total output noise is measured in  $\mu V(rms)$ .

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3853/LP3856 achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3853/LP3856 is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

#### SHORT-CIRCUIT PROTECTION

The LP3853 and LP3856 are short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

#### **ERROR FLAG OPERATION**

The LP3853/LP3856 produces a logic low signal at the Error Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in Figure 30 shows the relationship between the ERROR flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal  $\overline{\text{Error}}$  flag comparator has an <u>open drain</u> output stage. Hence, the  $\overline{\text{ERROR}}$  pin should be pulled high through a pull up resistor. Although the  $\overline{\text{ERROR}}$  flag pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of  $10\text{k}\Omega$  to  $1\text{M}\Omega$ . The  $\overline{\text{ERROR}}$  pin must be connected to ground if this function is not used. It should also be noted that when the shutdown pin is pulled low, the  $\overline{\text{ERROR}}$  pin is forced to be invalid for reasons of saving power in shutdown mode.



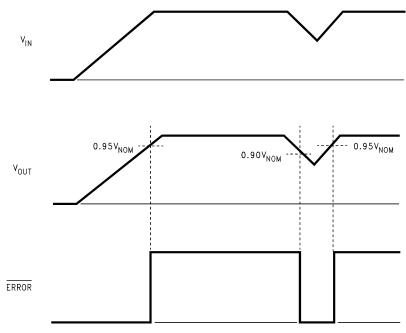


Figure 30. Error Flag Operation

#### **SENSE PIN**

In applications where the regulator output is not very close to the load, LP3856 can provide better remote load regulation using the SENSE pin. Figure 31 depicts the advantage of the SENSE option. LP3853 regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is  $100m\Omega$ , the voltage at the remote load will be 3V with 3A of load current, I<sub>LOAD</sub>. The LP3856 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 31. If the sense option pin is not required, the sense pin must be connected to the V<sub>OUT</sub> pin.

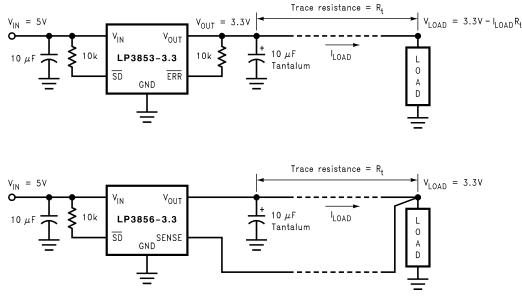


Figure 31. Improving remote load regulation using LP3856



#### SHUTDOWN OPERATION

A CMOS Logic low level signal at the Shutdown  $(\overline{SD})$  pin will turn-off the regulator. Pin  $\overline{SD}$  must be actively terminated through a  $10k\Omega$  pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

The Shutdown (SD) pin threshold has no voltage hysteresis. If the Shutdown pin is actively driven, the voltage transition must rise and fall cleanly and promptly.

#### **DROPOUT VOLTAGE**

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

#### **REVERSE CURRENT PATH**

The internal MOSFET in LP3853 and LP3856 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

#### POWER DISSIPATION/HEATSINKING

LP3853 and LP3856 can deliver a continuous current of 3A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$$

where I<sub>GND</sub> is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise  $(T_{Rmax})$  depends on the maximum ambient temperature  $(T_{Amax})$  of the application, and the maximum allowable junction temperature  $(T_{Jmax})$ :

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction to ambient Thermal Resistance,  $\theta_{JA}$ , can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_{D}$$

LP3853 and LP3856 are available in TO-220 and TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of  $\theta_{JA}$  calculated above is  $\geq$  60 °C/W for TO-220 package and  $\geq$  60 °C/W for TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable  $\theta_{JA}$  falls below these limits, a heat sink is required.

#### **HEATSINKING TO-220 PACKAGE**

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of  $\theta_{JA}$  will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \le \theta_{JA} - \theta_{CH} - \theta_{JC}$$
.

In this equation,  $\theta_{CH}$  is the thermal resistance from the case to the surface of the heat sink and  $\theta_{JC}$  is the thermal resistance from the junction to the surface of the case.  $\theta_{JC}$  is about 3°C/W for a TO220 package. The value for  $\theta_{CH}$  depends on method of attachment, insulator, etc.  $\theta_{CH}$  varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.



#### **HEATSINKING TO-263 PACKAGE**

The TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 32 shows a curve for the  $\theta_{JA}$  of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

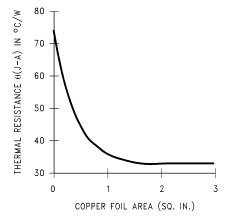


Figure 32.  $\theta_{JA}$  vs Copper (1 Ounce) Area for TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for  $\theta_{JA}$  for the TO-263 package mounted to a PCB is 32°C/W.

Figure 33 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming  $\theta_{JA}$  is 35°C/W and the maximum junction temperature is 125°C.

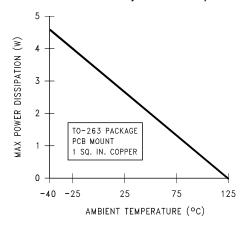


Figure 33. Maximum power dissipation vs ambient temperature for TO-263 package



## **REVISION HISTORY**

Cł	hanges from Revision F (April 2013) to Revision G	o Revision G Page			
•	Changed layout of National Data Sheet to TI format		16		

www.ti.com

23-May-2025

## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LP3853ES-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	Exempt SN Level-3-245C-168 HR -40 to 125		-40 to 125	LP3853ES -1.8
LP3853ES-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -1.8
LP3853ES-2.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -2.5
LP3853ES-2.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -2.5
LP3853ES-3.3/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -3.3
LP3853ES-3.3/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -3.3
LP3853ES-5.0/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -5.0
LP3853ES-5.0/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -5.0
LP3853ESX-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -1.8
LP3853ESX-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -1.8
LP3853ESX-2.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -2.5
LP3853ESX-2.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -2.5
LP3853ESX-3.3/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -3.3
LP3853ESX-3.3/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -3.3
LP3853ESX-5.0/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -5.0
LP3853ESX-5.0/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3853ES -5.0





23-May-2025 www.ti.com

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LP3853ET-1.8/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -1.8
LP3853ET-1.8/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -1.8
LP3853ET-2.5/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -2.5
LP3853ET-2.5/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -2.5
LP3853ET-3.3/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -3.3
LP3853ET-3.3/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -3.3
LP3853ET-5.0/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -5.0
LP3853ET-5.0/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3853ET -5.0
LP3856ES-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -1.8
LP3856ES-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -1.8
LP3856ES-2.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -2.5
LP3856ES-2.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -2.5
LP3856ES-3.3/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -3.3
LP3856ES-3.3/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -3.3
LP3856ES-5.0/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -5.0
LP3856ES-5.0/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -5.0
LP3856ESX-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -1.8





www.ti.com 23-May-2025

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LP3856ESX-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -1.8
LP3856ESX-2.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -2.5
LP3856ESX-2.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -2.5
LP3856ESX-3.3/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -3.3
LP3856ESX-3.3/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -3.3
LP3856ESX-5.0/NOPB	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -5.0
LP3856ESX-5.0/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP3856ES -5.0
LP3856ET-2.5/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -2.5
LP3856ET-2.5/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -2.5
LP3856ET-3.3/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -3.3
LP3856ET-3.3/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -3.3
LP3856ET-5.0/NOPB	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -5.0
LP3856ET-5.0/NOPB.A	Active	Production	TO-220 (NDH)   5	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP3856ET -5.0

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



## PACKAGE OPTION ADDENDUM

www.ti.com 23-May-2025

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com 23-May-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3853ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3853ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3853ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3853ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3856ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3856ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3856ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3856ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2



www.ti.com 23-May-2025



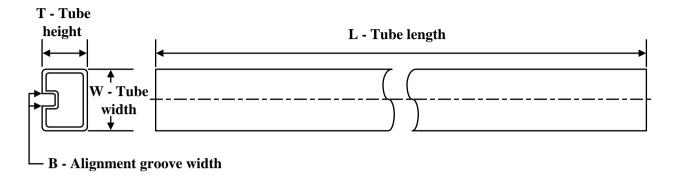
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3853ESX-1.8/NOPB	DDPAK/TO-263	КТТ	5	500	356.0	356.0	45.0
LP3853ESX-2.5/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3853ESX-3.3/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3853ESX-5.0/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3856ESX-1.8/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3856ESX-2.5/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3856ESX-3.3/NOPB	DDPAK/TO-263	ктт	5	500	356.0	356.0	45.0
LP3856ESX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0



www.ti.com 23-May-2025

## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP3853ES-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-1.8/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-2.5/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-2.5/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-3.3/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-3.3/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-5.0/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ES-5.0/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3853ET-1.8/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-1.8/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-2.5/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-2.5/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-3.3/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-3.3/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-5.0/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3853ET-5.0/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3856ES-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-1.8/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-2.5/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-2.5/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-3.3/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-3.3/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-5.0/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ES-5.0/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3856ET-2.5/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3856ET-2.5/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3856ET-3.3/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3856ET-3.3/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74
LP3856ET-5.0/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74



## PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP3856ET-5.0/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74





#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated