





TEXAS INSTRUMENTS

SN74HC11, SN54HC11 SCLS084E – DECEMBER 1982 – REVISED APRIL 2021

(1)

...

# SNx4HC11 Triple 3-Input AND Gates

## 1 Features

- · Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Wide operating temperature range: -40°C to +85°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

## 2 Applications

- Combining power good signals
- Enable digital signals

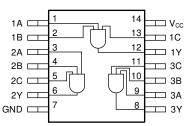
## **3 Description**

This device contains three independent 3-input AND gates. Each gate performs the Boolean function  $Y = A \bullet B \bullet C$  in positive logic.

. .

Device Information <sup>(1)</sup>								
PART NUMBER	PACKAGE	BODY SIZE (NOM)						
SN74HC11DR	SOIC (14)	8.70 mm × 3.90 mm						
SN74HC11NR	PDIP (14)	19.30 mm × 6.40 mm						
SN74HC11NSR	SO (14)	10.20 mm × 5.30 mm						
SN74HC11PWR	TSSOP (14)	5.00 mm × 4.40 mm						
SN54HC11JR	CDIP (14)	21.30 mm × 7.60 mm						
SN54HC11WR	CFP (14)	9.20 mm × 6.29 mm						
SN54HC11FKR	LCCC (20)	8.90 mm × 8.90 mm						
	1	1						

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Functional pinout** 



## **Table of Contents**

1 Features	1
2 Applications	
3 Description	1
4 Revision History	
5 Pin Configuration and Functions	3
Pin Functions	3
6 Specifications	4
6.1 Absolute Maximum Ratings	
6.2 Recommended Operating Conditions	4
6.3 Thermal Information	
6.4 Electrical Characteristics - 74	5
6.5 Electrical Characteristics - 54	5
6.6 Switching Characteristics - 74	6
6.7 Switching Characteristics - 54	6
6.8 Operating Characteristics	6
6.9 Typical Characteristics	6
7 Parameter Measurement Information	8
8 Detailed Description	9
8.1 Overview	

8.2 Functional Block Diagram	9
8.3 Feature Description.	
8.4 Device Functional Modes	
9 Application and Implementation	
9.1 Application Information	
9.2 Typical Application	
10 Power Supply Recommendations	
11 Layout	
11.1 Layout Guidelines	13
11.2 Layout Example	13
12 Device and Documentation Support	
12.1 Documentation Support	
12.2 Related Links	
12.3 Support Resources	
12.4 Trademarks	14
12.5 Electrostatic Discharge Caution	14
12.6 Glossary	
13 Mechanical, Packaging, and Orderable	
Information	14

## **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision D (August 2003) to Revision E (April 2021)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Updated to new data sheet standards	1
•	Increased thermals for D, PW and NS packages and decreased N package thermals	4



## **5** Pin Configuration and Functions

1A 🗆	1 🔿	14	
1B 🗖	2	13	1C
2A 🗖	3	12	💷 1Y
2B 🗖	4	11	3C
2C 🗖	5	10	🗔 ЗВ
2Y 🗖	6	9	🗔 3A
GND 🖂	7	8	3Y

#### Figure 5-1. D, N, NS, PW, J, or W Package 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, or CFP Top View

		1B	1A	NC	$V_{\text{CC}}$	1C	
	0	3	2	1	20	19	
2A	∷4					18 🕮	1Y
NC	∷:5					17 🗆	NC
2B	∷:6					16∷	3C
NC	∷:7					15∷	NC
2C	∷8					14 🕮	3B
		9	10	11 П	12 m	13 m	
	2	2Y (	GND	) NC	3Y	ЗA	
Fia	<b>r</b>	- F	5_2	E	K P	acka	ane

Figure 5-2. FK Package 20-Pin LCCC Top View

#### **Pin Functions**

PIN								
NAME	D, N, NS, PW, J, or W	FK	I/O	DESCRIPTION				
1A	1	2	Input	Channel 1, Input A				
1B	2	3	Input	Channel 1, Input B				
2A	3	4	Input	Channel 2, Input A				
2B	4	6	Input	Channel 2, Input B				
2C	5	8	Input	Channel 2, Input C				
2Y	6	9	Output	Channel 2, Output Y				
GND	7	10	_	Ground				
3Y	8	12	Output	Channel 3, Output Y				
3A	9	13	Input	Channel 3, Input A				
3B	10	14	Input	Channel 3, Input B				
3C	11	16	Input	Channel 3, Input C				
1Y	12	18	Output	Channel 1, Output Y				
1C	13	19	Input	Channel 1, Input C				
V <sub>CC</sub>	14	20	_	Positive Supply				
NC		1, 5, 7, 11, 15, 17	_	Not internally connected				



# 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$V_{I} < 0 V \text{ or } V_{I} > V_{CC}$		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$V_{O}$ < 0 V or $V_{O}$ > $V_{CC}$		±20	mA
Io	Continuous output current	$V_{O} = 0$ to $V_{CC}$		±25	mA
	Continuous current through $V_{CC}$ or GND			±50	mA
TJ	Junction temperature <sup>(3)</sup>		150	°C	
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	·	2	5	6	V	
		V <sub>CC</sub> = 2 V	1.5				
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			V	
		V <sub>CC</sub> = 6 V	4.2				
		V <sub>CC</sub> = 2 V			0.5		
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35	V	
		V <sub>CC</sub> = 6 V			1.8		
VI	Input voltage		0		V <sub>CC</sub>	V	
Vo	Output voltage		0		V <sub>CC</sub>	V	
		V <sub>CC</sub> = 2 V			1000		
Δt/Δv	Input transition rise and fall rate	V <sub>CC</sub> = 4.5 V			500	ns	
		V <sub>CC</sub> = 6 V			400	1	
Ŧ	Operating free air temperature	SN54HC00	-55		125	°C	
T <sub>A</sub>	Operating free-air temperature	SN74HC00	-40		85	C	

#### 6.3 Thermal Information

	THERMAL METRIC <sup>(1)</sup>		N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta J A}$	Junction-to-ambient thermal resistance	133.6	65.2	122.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.0	52.9	81.8	79.4	°C/W
$R_{\theta J B}$	Junction-to-board thermal resistance	89.5	44.9	83.8	94.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	45.5	32.5	45.4	25.2	°C/W



THERMAL METRIC <sup>(1)</sup>		D (SOIC)	D (SOIC) N (PDIP)		PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	89.1	44.7	83.4	94.1	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.4 Electrical Characteristics - 74

over operating free-air temperature range; typical values measured at  $T_A = 25^{\circ}C$  (unless otherwise noted).

		TEST CONDITIONS			Operating free-air temperature (T <sub>A</sub> )						
F	PARAMETER			V <sub>cc</sub>		25°C			-40°C to 85°C		
					MIN	TYP	MAX	MIN	TYP	MAX	
				2 V	1.9	1.998		1.9			
		., .,	I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4			
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		6 V	5.9	5.999		5.9			V
			I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.84			
			I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.34			
		$V_I = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1			0.1	
				4.5 V		0.001	0.1			0.1	
V <sub>OL</sub>	Low-level output voltage			6 V		0.001	0.1			0.1	V
			I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26			0.33	
			I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26			0.33	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> c	or O	6 V			±0.1			±1	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0	I <sub>O</sub> = 0	6 V			2			20	μA
Ci	Input capacitance			2 V to 6 V		3	10			10	pF

### 6.5 Electrical Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

	1 0		<u> </u>				Opera	ting free	air tem-	peratur	e (T <sub>A</sub> )			
I	PARAMETER	TEST CO	NDITIONS	V <sub>cc</sub>		25°C		–40°	C to 85	°C	–55°(	C to 125	5°C	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
				2 V	1.9	1.998		1.9			1.9			
			I <sub>OH</sub> = –20 μΑ	4.5 V	4.4	4.499		4.4			4.4			
	High-level	V <sub>I</sub> = V <sub>IH</sub> or	<b>F</b> <sup></sup> <b>F</b>	6 V	5.9	5.999		5.9			5.9			.,
V <sub>OH</sub>	output voltage	V <sub>IL</sub>	I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3								V
			I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8								
				2 V		0.002	0.1			0.1			0.1	
			I <sub>OL</sub> = 20 μΑ	4.5 V		0.001	0.1			0.1			0.1	
VOL			<b>F</b> <sup>2</sup> <b>F</b> <sup>2</sup>	6 V		0.001	0.1			0.1			0.1	v
	voltage	VIL	$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26			0.33			0.4	
			I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26			0.33			0.4	

Copyright © 2021 Texas Instruments Incorporated

#### SN74HC11, SN54HC11 SCLS084E – DECEMBER 1982 – REVISED APRIL 2021



#### over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

					Operating free-air temperature (T <sub>A</sub> )									
	PARAMETER	TEST CO	NDITIONS	V <sub>cc</sub>	25°C		–40°C to 85°C			–55°C to 125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I <sub>I</sub>	current	$V_{I} = V_{CC}$ or		6 V			±0.1			±1			±1	μA
I <sub>CC</sub>	Supply current	$V_{I} = V_{CC}$ or 0	I <sub>O</sub> = 0	6 V			2			20			40	μA
Ci	Input capacitance			2 V to 6 V		3	10			10			10	pF

### 6.6 Switching Characteristics - 74

over operating free-air temperature range (unless otherwise noted)

					Op						
	PARAMETER	FROM	то	V <sub>cc</sub>	25°C			–40°C to 85°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
				2 V		35	100			125	
t <sub>pd</sub>	Propagation delay	A, B, or C	Y	4.5 V		10	20			25	ns
				6 V		8	17			21	
				2 V		25	75			95	
tt	Transition-time		Y	4.5 V		7	15			19	ns
				6 V		5	13			16	

#### 6.7 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

								C	Operati	ng free	-air ten	nperatu				
	PARAMETER	FROM	то	то	то	V <sub>cc</sub>		25°C		–40°C to 85°C			–55°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
				2 V		35	100			125			150			
t <sub>pd</sub>	Propagation delay	A, B, or C	Y	4.5 V		10	20			25			30	ns		
				6 V		8	17			21			25			
				2 V		25	75			95			110			
tt	Transition-time		Y	4.5 V		7	15			19			22	ns		
				6 V		5	13			16			19	1		

#### 6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^{\circ}C$  (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP MA	K UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	No load	2 V to 6 V		25	pF

### **6.9 Typical Characteristics**

T<sub>A</sub> = 25°C



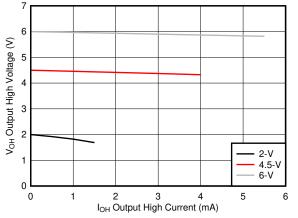


Figure 6-1. Typical output voltage in the high state  $$(V_{OH})$$ 

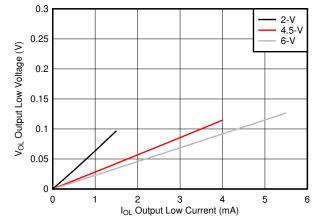
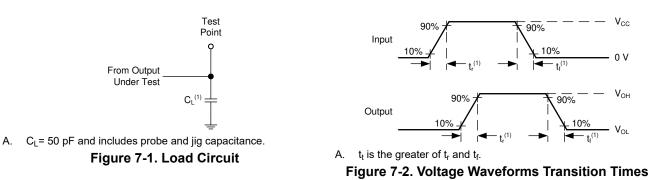


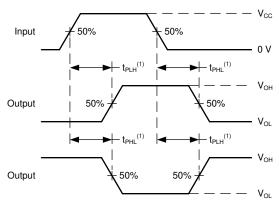
Figure 6-2. Typical output voltage in the low state  $$(V_{\text{OL}})$$ 



### 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>t</sub> < 6 ns.</li>
- The outputs are measured one at a time, with one input transition per measurement.





A. The maximum between  $t_{\mathsf{PLH}}$  and  $t_{\mathsf{PHL}}$  is used for  $t_{\mathsf{pd}}.$ 

#### Figure 7-3. Voltage Waveforms Propagation Delays

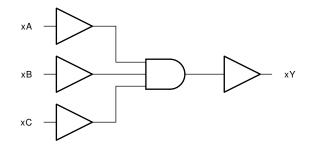


### 8 Detailed Description

### 8.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

#### 8.2 Functional Block Diagram



#### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC11 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics* - 74 connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics* - 74. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics* - 74, using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

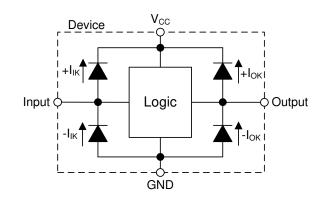


#### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 8-1.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



#### Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

#### 8.4 Device Functional Modes

	INPUTS		OUTPUT
Α	В	С	Y
н	Н	Н	Н
L	Х	Х	L
Х	L	Х	L
Х	Х	L	L

#### Table 8-1. Function Table



### **9** Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 9.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

#### 9.2 Typical Application

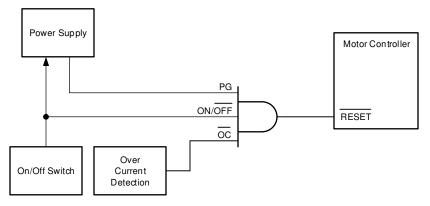


Figure 9-1. Typical application schematic

#### 9.2.1 Design Requirements

#### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* - 74.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC11 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics* - 74. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and  $C_{pd}$  Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

#### CAUTION

The maximum junction temperature,  $T_J(max)$  listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.



#### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC11, as specified in the *Electrical Characteristics* - 74, and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HC11 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to Section 8.3 for additional information regarding the inputs for this device.

#### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics* - 74. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics* - 74.

Unused outputs can be left floating. Do not connect outputs directly to V<sub>CC</sub> or ground.

Refer to Section 8.3 for additional information regarding the outputs for this device.

#### 9.2.2 Detailed Design Procedure

- 1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in *Section 11*.
- Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal
  performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC11
  to the receiving device.
- Ensure the resistive load at the output is larger than (V<sub>CC</sub> / I<sub>O</sub>(max)) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
- 4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

#### 9.2.3 Application Curves

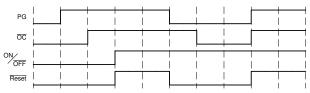


Figure 9-2. Typical application timing diagram



### **10 Power Supply Recommendations**

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 11-1*.

### 11 Layout

#### **11.1 Layout Guidelines**

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

#### 11.2 Layout Example

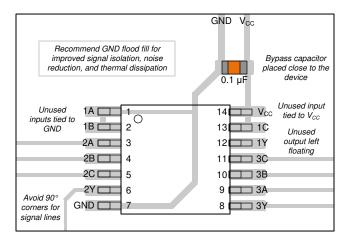


Figure 11-1. Example layout for the SN74HC11



### 12 Device and Documentation Support

### **12.1 Documentation Support**

#### 12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

#### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

#### **12.3 Support Resources**

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 12.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8404801VCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8404801VC A SNV54HC11J
5962-8404801VCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8404801VC A SNV54HC11J
84048012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84048012A SNJ54HC 11FK
8404801CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801CA SNJ54HC11J
8404801DA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801DA SNJ54HC11W
JM38510/65204BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65204BCA
JM38510/65204BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65204BCA
M38510/65204BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65204BCA
SN54HC11J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC11J
SN54HC11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC11J
SN74HC11D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HC11
SN74HC11DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11DR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11DR1G4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11DR1G4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11DT	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HC11
SN74HC11DT.B	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HC11
SN74HC11N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC11N
SN74HC11N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC11N
SN74HC11NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11



24-Jul-2025

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74HC11NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HC11
SN74HC11PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11PWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SN74HC11PWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC11
SNJ54HC11FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84048012A SNJ54HC 11FK
SNJ54HC11FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84048012A SNJ54HC 11FK
SNJ54HC11J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801CA SNJ54HC11J
SNJ54HC11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801CA SNJ54HC11J
SNJ54HC11W	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801DA SNJ54HC11W
SNJ54HC11W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801DA SNJ54HC11W

<sup>(1)</sup> **Status:** For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



www.ti.com

# PACKAGE OPTION ADDENDUM

24-Jul-2025

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HC11, SN54HC11-SP, SN74HC11 :

• Catalog : SN74HC11, SN54HC11

• Military : SN54HC11

• Space : SN54HC11-SP

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



Texas

STRUMENTS

### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



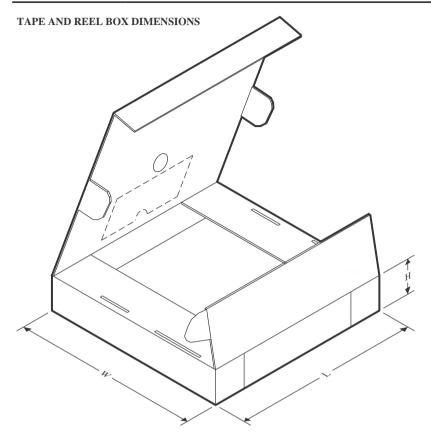
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC11DR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC11NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC11PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC11PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



www.ti.com

# PACKAGE MATERIALS INFORMATION

2-Aug-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC11DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74HC11DR1G4	SOIC	D	14	2500	353.0	353.0	32.0
SN74HC11NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HC11PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HC11PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

### TEXAS INSTRUMENTS

www.ti.com

2-Aug-2025

## TUBE



## - B - Alignment groove width

*All dimensions	are nominal
-----------------	-------------

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
84048012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8404801DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74HC11N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC11N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC11N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC11N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HC11FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC11FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC11W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54HC11W.A	W	CFP	14	25	506.98	26.16	6220	NA

# **D0014A**



# **PACKAGE OUTLINE**

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



# D0014A

# **EXAMPLE BOARD LAYOUT**

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# D0014A

# **EXAMPLE STENCIL DESIGN**

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### MECHANICAL DATA

### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14



# FK 20

### 8.89 x 8.89, 1.27 mm pitch

# **GENERIC PACKAGE VIEW**

## LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





# **GENERIC PACKAGE VIEW**

# CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



# J0014A



# **PACKAGE OUTLINE**

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



# J0014A

# **EXAMPLE BOARD LAYOUT**

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE





# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



# **PW0014A**



# **PACKAGE OUTLINE**

# TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



# PW0014A

# **EXAMPLE BOARD LAYOUT**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# PW0014A

# **EXAMPLE STENCIL DESIGN**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



<sup>8.</sup> Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated