







**SN54HCT32, SN74HCT32** 

SCLS064G - NOVEMBER 1988 - REVISED OCTOBER 2022

# **SNx4HCT32 Quadruple 2-Input Positive-OR Gates**

## 1 Features

- Operating voltage range of 4.5 V to 5.5 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 20-µA max I<sub>CC</sub>
- Typical  $t_{pd}$  = 13 ns
- ±4-mA output drive at 5 V
- Low input current of 1 µA max
- Inputs are TTL-Voltage compatible

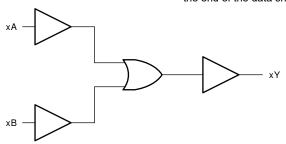
## 2 Description

The SNx4HCT32 device contains four independent 2-input OR gates. They perform the Boolean function Y = A + B in positive logic.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74HCT32D	SOIC (14)	8.65 mm × 3.90 mm
SN74HCT32DBR	SSOP (14)	6.20 mm × 5.30 mm
SN74HCT32N	PDIP (14)	19.31 mm × 6.35 mm
SN74HCT32NSR	SO (14)	10.20 mm × 5.30 mm
SN74HCT32PW	TSSOP (14)	5.00 mm × 4.40 mm

For all available packages, see the orderable addendum at the end of the data sheet.



**Functional Block Diagram** 



## **Table of Contents**

1 Features	1	7.2 Functional Block Diagram	. 7
2 Description		7.3 Device Functional Modes	.7
3 Revision History		8 Power Supply Recommendations	3.
4 Pin Configuration and Functions	3	9 Layout	
5 Specifications		9.1 Layout Guidelines	
5.1 Absolute Maximum Ratings	4	10 Device and Documentation Support	.0
5.2 Recommended Operating Conditions (1)	4	10.1 Documentation Support	
5.3 Thermal Information	4	10.2 Receiving Notification of Documentation Updates	. 9
5.4 Electrical Characteristics	5	10.3 Support Resources	
5.5 Switching Characteristics	5	10.4 Trademarks	
5.6 Operating Characteristics	5	10.5 Electrostatic Discharge Caution	. 9
6 Parameter Measurement Information	6	10.6 Glossary	
7 Detailed Description	7	11 Mechanical, Packaging, and Orderable	
7.1 Overview	7	Information	ę
O Davisian History			
3 Revision History			

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision F (February 2022) to Revision G (October 2022)

**Page** 

Increased R0JA for packages: D (86 to 138.7); DB (96 to 114.8); N (80 to 67); NS (76 to 93.3); PW (113 to 159.8)......4

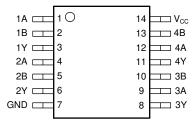
## Changes from Revision E (August 2003) to Revision F (February 2022)

Page

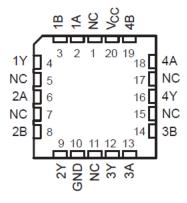
Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards......1



# **4 Pin Configuration and Functions**



D, DB, N, NS, PW Package 14-Pin SOIC, SSOP, PDIP, SO, TSSOP Top View



NC - No internal connection

FK package 20-Pin LCCC Top View



## **5 Specifications**

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$(V_1 < 0 \text{ or } V_1 > V_{CC})$		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25	mA
V <sub>CC</sub> or GND	Continuous current through			±50	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 5.2 Recommended Operating Conditions<sup>(1)</sup>

			SN54HCT32 <sup>(2)</sup>			SN	UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2			2	,		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			0.8	V
VI	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Vo	Output voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition rise/fall time				500			500	ns
T <sub>A</sub>	Operating free-air temperature		- 55		125	- 40		85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

#### 5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
THERMAL	. METRIC	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	138.7	114.8	67	93.3	159.8	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	93.8	60	55	50.9	92.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	63.8	46.7	53.8	102.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	49.1	19.7	35.1	17.8	40.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	94.3	63.1	46.5	53.3	101.7	°C/W
R <sub>θJC (bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> SN54HCT32 is in product preview.

## **5.4 Electrical Characteristics**

	PARAMETER	TEST CONDITIONS(1)	V <sub>cc</sub>	T,	<sub>A</sub> = 25°C		SN54HC	CT32 <sup>(3)</sup>	SN74HCT32		UNIT
	PARAIVIETER	TEST CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -20 μA	4.5	4.4	4.499		4.4		4.4		V
V OH	i ligii-level output voltage	I <sub>OH</sub> = -4 mA	4.5	3.98	4.3		3.7		3.84		V
V	Low-level output voltage	I <sub>OL</sub> = 20 μA	4.5		0.001	0.1		0.1		0.1	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA	4.5		0.17	0.26		0.4		0.33	V
II	Input hold current	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5		±0.1	±100		±1000		±1000	nA
Icc	Supply current	$V_I = V_{CC}$ or 0. $I_O = 0$	5.5			2		40		20	μΑ
ΔI <sub>CC</sub> <sup>(2)</sup>	Supply-current change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5		1.4	2.4		3		2.9	mA
Ci	Input capacitance		4.5 to 5.5		3	10		10		10	pF

- (1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.
   (2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.
- (3) SN54HCT32 is in product preview.

## **5.5 Switching Characteristics**

 $C_L$  = 50 pF. See Parameter Measurement Information.

	PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub>		T <sub>A</sub> = 25°C			T32 <sup>(1)</sup>	SN74HCT32	
	PARAMETER	(INPUT)	10 (001701)	(V)	MIN	TYP	MAX	MIN	MAX	MIN MAX	3
+ .	t <sub>pd</sub> Propagation delay A c	A or B	Y	4.5		15	24		35	30	ns
<sup>L</sup> pd		AOIB		5.5		13	22		32	27	
	Transition time	V	4.5		9	15		22	19		
ч			ř	5.5		8	14		20	17	ns

<sup>(1)</sup> SN54HCT32 device is in product preview.

## **5.6 Operating Characteristics**

 $T_A = 25^{\circ}C$ 

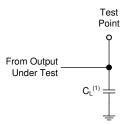
		Test Conditions	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	20	pF

## **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_t$  < 6 ns.

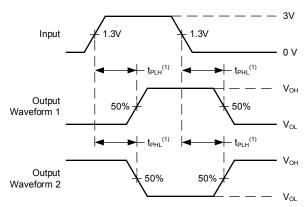
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

Figure 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

# 7 Detailed Description

## 7.1 Overview

The SN74HCT32 devices contain four independent 2-input OR gates. They perform the Boolean function Y = A + B in positive logic.

# 7.2 Functional Block Diagram

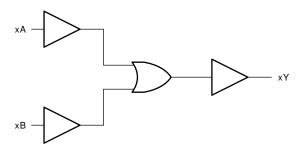


Figure 7-1. Functional Block Diagram

## 7.3 Device Functional Modes

Table 7-1. Function Table (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Х	Н
Х	Н	Н
L	L	L

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## **10.1 Documentation Support**

#### 10.1.1 Related Documentation

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 31-Oct-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74HCT32DBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT32
SN74HCT32DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT32
SN74HCT32DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32DRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32DT	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HCT32
SN74HCT32N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT32N
SN74HCT32N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT32N
SN74HCT32NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT32
SN74HCT32PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HT32
SN74HCT32PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HT32
SN74HCT32PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT32
SN74HCT32PWR1G4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT32
SN74HCT32PWT	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HT32

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT32DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT32DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT32NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCT32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT32PWR1G4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT32PWR1G4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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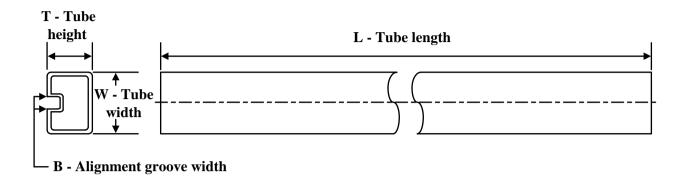
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT32DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74HCT32DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74HCT32DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT32NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCT32PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT32PWR1G4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT32PWR1G4	TSSOP	PW	14	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 19-Sep-2025

## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HCT32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT32N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT32N.A	N	PDIP	14	25	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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