# Isolated, Dual Channel, RS-232 Line Driver/Receiver

Data Sheet

# ADM3252E

## FEATURES

- 2.5 kV fully isolated (power and data) RS-232 transceiver
- *iso*Power integrated, isolated dc-to-dc converter
- Operational from single 3.3 V or 5 V supply
- 460 kbps data rate
- 2 × Tx and 2 × Rx channels
- Meets EIA/TIA-232E specifications
- ESD protection to IEC 61000-4-2 on $R_{INx}$ and $T_{OUTx}$ pins
  - Contact discharge: ±8 kV
  - Air gap discharge: ±15 kV
- 0.1 µF charge pump capacitors
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals (pending)
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - VDE certificate of conformity
    - IEC 60747-5-2 (VDE 0884, Part 2)
    - $V_{IORM}$ = 560 V peak
  - CSA Component Acceptance Notice #5A
- Operating temperature range: −40°C to +85°C
- 44-ball chip scale package ball grid array (CSP_BGA)

## APPLICATIONS

- Isolated RS-232 interface
- High noise data communications
- Industrial communications
- Industrial/telecommunications diagnostic ports
- Medical equipment

## FUNCTIONAL BLOCK DIAGRAM

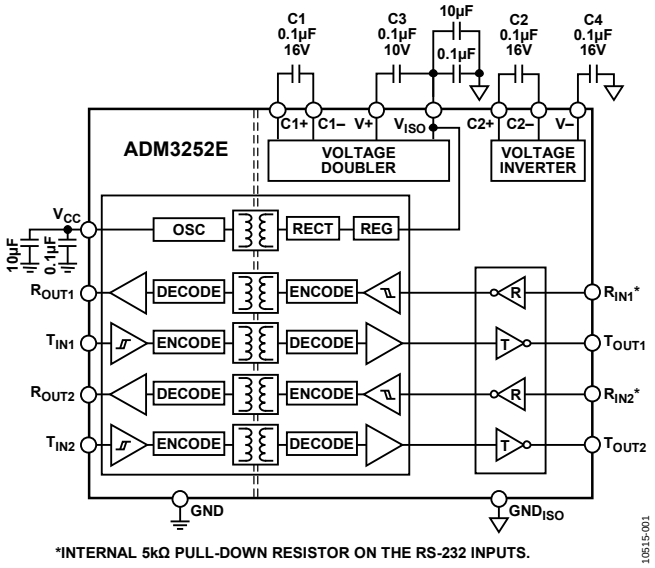


*Figure 1.*

## GENERAL DESCRIPTION

The ADM3252E is a high speed, 2.5 kV, fully isolated, dual-channel RS-232/V.28 transceiver device that is operational from a single 3.3 V or 5 V power supply. Because of high ESD protection on the $R_{IN1}$, $R_{IN2}$, $T_{OUT1}$, and $T_{OUT2}$ pins, the ADM3252E is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently plugged and unplugged.

The ADM3252E provides four independent isolation channels using the integrated and isolated power of *iso*Power™. There is no requirement to use a separate isolated dc-to-dc converter. Chip scale transformer *i*Coupler® technology from Analog Devices, Inc., is used for both the isolation of the logic signals and the integrated dc-to-dc converter. The result is a total isolation solution.

*iso*Power technology in the ADM3252E uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*, for details on board layout considerations.

The ADM3252E conforms to the EIA/TIA-232E and ITU-T V.28 specifications and operates at data rates of up to 460 kbps. Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter, permitting operation from a single 3.3 V or 5 V supply. The ADM3252E is available in a 44-ball, chip scale package ball grid array (CSP_BGA) and is specified over the −40°C to +85°C temperature range.

Rev. A
Document Feedback


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**1/13—Rev. 0 to Rev. A**

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Changes to Figure 20 ... 12

**4/12—Revision 0: Initial Version**

# SPECIFICATIONS

All voltages are relative to their respective grounds, all minimum/maximum specifications apply over the entire recommended operating range, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DC CHARACTERISTICS | | | | | |
| $V_{CC}$ Operating Voltage Range | 3.0 | 3.3 | 5.5 | V | |
| UVLO Threshold | | | | | |
| Rising | | 2.7 | | V | Undervoltage lockout |
| Falling | | 2.3 | | V | |
| Input Supply Current, $I_{CC}$ | | 20 | 35 | mA | No load |
| | | 45 | 75 | mA | $R_L$ = 3 kΩ, $V_{CC}$ = 3.0 V to 5.5 V |
| | | 35 | 60 | mA | $R_L$ = 3 kΩ, $V_{CC}$ = 3.3 V |
| $V_{ISO}$ Output | | 3.3 | | V | $I_{ISO}$ = 0 µA |
| $V_{ISO}$ Maximum Load Current, $I_{ISO(MAX)}$ | | | 15 | mA | |
| LOGIC | | | | | |
| Transmitter Inputs, $T_{IN1}$ and $T_{IN2}$ | | | | | |
| Logic Input Current | −10 | +0.01 | +10 | µA | |
| Logic Input Threshold | | | | | |
| Low | | | 0.3 × $V_{CC}$ | V | |
| High | 0.7 × $V_{CC}$ | | | V | |
| Receiver Outputs, $R_{OUT1}$ and $R_{OUT2}$ | | | | | |
| Logic High Output | $V_{CC}$ − 0.2 | $V_{CC}$ | | V | $I_{ROUTH}$ = −20 µA |
| | $V_{CC}$ − 0.5 | $V_{CC}$ − 0.3 | | V | $I_{ROUTH}$ = −4 mA |
| Logic Low Output | | 0.0 | 0.1 | V | $I_{ROUTH}$ = 20 µA |
| | | 0.2 | 0.4 | V | $I_{ROUTH}$ = 4 mA |
| RS-232 | | | | | |
| Receiver Inputs, $R_{IN1}$ and $R_{IN2}$ | | | | | |
| EIA-232 Input | | | | | |
| Voltage Range[1] | −30 | | +30 | V | |
| Threshold Low | 0.8 | 1.0 | | V | |
| Threshold High | | 1.5 | 2.0 | V | |
| Hysteresis | | 0.45 | | V | |
| Resistance | 3 | 5 | 7 | kΩ | |
| Transmitter Outputs, $T_{OUT1}$ and $T_{OUT2}$ | | | | | |
| Output Voltage Swing (RS-232) | ±5.0 | ±5.2 | | V | $R_L$ = 3 kΩ to GND |
| Transmitter Output Resistance | 300 | | | Ω | $V_{CC}$ = 0 V, $V_{ISO}$ = 0 V |
| Output Short-Circuit Current (RS-232) | | ±15 | | mA | |
| TIMING CHARACTERISTICS | | | | | |
| Maximum Data Rate | 460 | | | kbps | $R_L$ = 3 kΩ to 7 kΩ, $C_L$ = 50 pF to 1000 pF |
| Receiver Propagation Delay | | | | | |
| $t_{PHL}$ | | 0.4 | 1 | µs | |
| $t_{PLH}$ | | 0.4 | 1 | µs | |
| Transmitter Propagation Delay | | 0.3 | 1.2 | µs | $R_L$ = 3 kΩ, $C_L$ = 1000 pF |
| Transmitter Skew | | 30 | | ns | |
| Receiver Skew | | 300 | | ns | |
| Transition Region Slew Rate | | 10 | | V/µs | Measured from +3 V to −3 V or −3 V to +3 V, $V_{CC}$ = +3.3 V, $R_L$ = 3 kΩ, $C_L$ = 1000 pF, $T_A$ = 25°C |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| AC SPECIFICATIONS | | | | | |
| Output Rise/Fall Time, $t_R/t_F$ (10% to 90%) | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity | | | | | |
| Logic High Output[2] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| Logic Low Output[2] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| Refresh Rate | | 1.0 | | Mbps | |

[1] Guaranteed by design.
[2] $V_{CM}$ is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. $V_{CM}$ is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode voltage is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode edges.

## PACKAGE CHARACTERISTICS

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| PACKAGE CHARACTERISTICS | | | | | | |
| Resistance (Input-to-Output) | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input-to-Output) | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | | 40 | | °C/W | |

## REGULATORY INFORMATION (PENDING)

**Table 3.**

| UL | CSA | VDE |
|---|---|---|
| Recognized Under UL 1577 Component Recognition Program[1] | Approved under CSA Component Acceptance Notice #5A | Certified according to IEC 60747-5-2 (VDE 0884 Part 2):2003-01[2] |
| Single Protection, 2500 V rms Isolation Voltage | Testing was conducted per CSA 60950-1-07 and IEC 60950-1 2nd ed. at 2.5 kV rated voltage<br>Basic insulation at 400 V rms (565 V peak) working voltage | Basic insulation, 560 V peak |

[1] In accordance with UL 1577, each ADM3252E is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 15 µA).
[2] In accordance with IEC 60747-5-2 (VDE 0884 Part 2):2003-01, each ADM3252E is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates IEC 60747-5-2 (VDE 0884 Part 2):2003-01 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 4.**

| Parameter | Symbol | Value | Unit | Test Conditions |
|---|---|---|---|---|
| INSULATION AND SAFETY | | | | |
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1 minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.6 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 7.6 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 | mm | Distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | |
| Isolation Group | | IIIa | | |

## ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| $V_{CC}$, $V_{ISO}$ | −0.3 V to +6 V |
| V+ | ($V_{CC}$ − 0.3 V) to +13 V |
| V− | −13 V to +0.3 V |
| Input Voltages | |
| $T_{IN1}$, $T_{IN2}$ | −0.3 V to ($V_{CC}$ + 0.3 V) |
| $R_{IN1}$, $R_{IN2}$ | ±30 V |
| Output Voltages | |
| $T_{OUT1}$, $T_{OUT2}$ | ±15 V |
| $R_{OUT1}$, $R_{OUT2}$ | −0.3 V to ($V_{CC}$ + 0.3 V) |
| Short-Circuit Duration | |
| $T_{OUT1}$, $T_{OUT2}$ | Continuous |
| Power Dissipation | 750 mW |
| Operating Temperature Range | |
| Industrial | −40°C to +85°C |
| Storage Temperature | −65°C to +150°C |
| Pb-Free Temperature (Soldering, 30 sec) | 260°C |
| Storage Temperature Prior to Soldering | 30°C/60% RH max for 168 hours (MSL3) |
| Bake Temperature (If Required) | 125°C + 5°C/−0°C for 48 hours |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

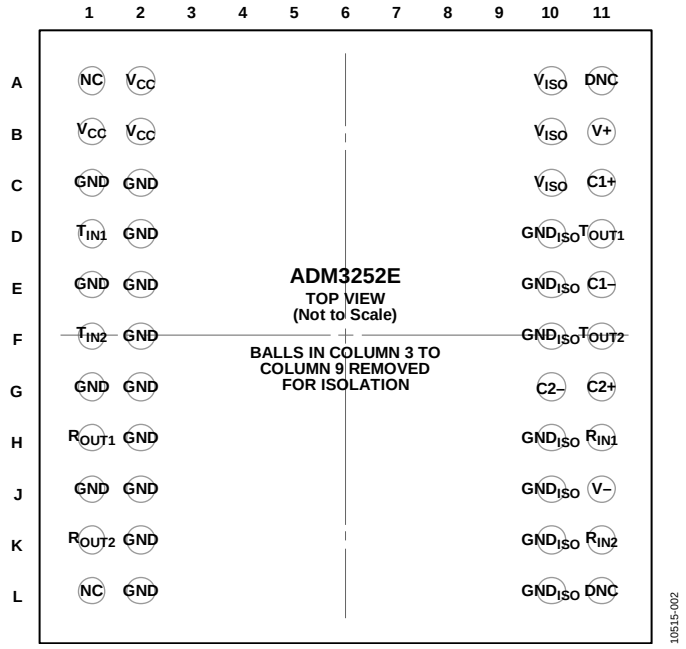



*Figure 2. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1, L1 | NC | No Connect. These pins are left unconnected. |
| A2, B1, B2 | $V_{CC}$ | Power Supply Input. A 10 µF and a 0.1 µF decoupling capacitor are required between $V_{CC}$ and ground. The device requires a voltage between 3.0 V and 5.5 V. |
| A10, B10, C10 | $V_{ISO}$ | Supply Voltage for Isolator Secondary Side. A 10 µF and a 0.1 µF decoupling capacitor are required between $V_{ISO}$ and ground. |
| A11, L11 | DNC | Do Not Connect. Do not connect or route anything through these pins. |
| B11 | V+ | Internally Generated Positive Supply. |
| C1, C2, D2, E1, E2, F2, G1, G2, H2, J1, J2, K2, L2 | GND | Ground Reference for Logic Side. |
| C11, E11, G10, G11 | C1+, C1−, C2−, C2+ | Positive and Negative Connections for Charge Pump Capacitors. External Capacitors C1 and C2 are connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors of up to 10 µF can be used. |
| D1 | $T_{IN1}$ | Transmitter (Driver) Input 1. A logic low on this input generates a high on $T_{OUT1}$; a logic high on this input generates a low on $T_{OUT1}$. This pin accepts TTL/CMOS levels. This is a high impedance input pin; therefore, it should not be left floating. |
| D10, E10, F10, H10, J10, K10, L10 | $GND_{ISO}$ | Ground Reference for Isolated RS-232 Side. |
| D11 | $T_{OUT1}$ | Transmitter (Driver) Output 1. This pin outputs RS-232 signal levels. |
| F1 | $T_{IN2}$ | Transmitter (Driver) Input 2. A logic low on this input generates a high on $T_{OUT2}$; a logic high on this input generates a low on $T_{OUT2}$. This pin accepts TTL/CMOS levels. This is a high impedance input pin; therefore, it should not be left floating. |
| F11 | $T_{OUT2}$ | Transmitter (Driver) Output 2. This pin outputs RS-232 signal levels. |
| H1 | $R_{OUT1}$ | Receiver Output 1. This pin outputs CMOS logic levels. |
| H11 | $R_{IN1}$ | Receiver Input 1. A logic low on this input generates a high on $R_{OUT1}$; a logic high on this input generates a low on $R_{OUT1}$. This input pin accepts RS-232 signal levels and has an internal 5 kΩ pull-down resistor. |
| J11 | V− | Internally Generated Negative Supply. |
| K1 | $R_{OUT2}$ | Receiver Output 2. This pin outputs CMOS logic levels. |
| K11 | $R_{IN2}$ | Receiver Input 2. A logic low on this input generates a high on $R_{OUT2}$; a logic high on this input generates a low on $R_{OUT2}$. This input pin accepts RS-232 signal levels and has an internal 5 kΩ pull-down resistor. |

# TYPICAL PERFORMANCE CHARACTERISTICS

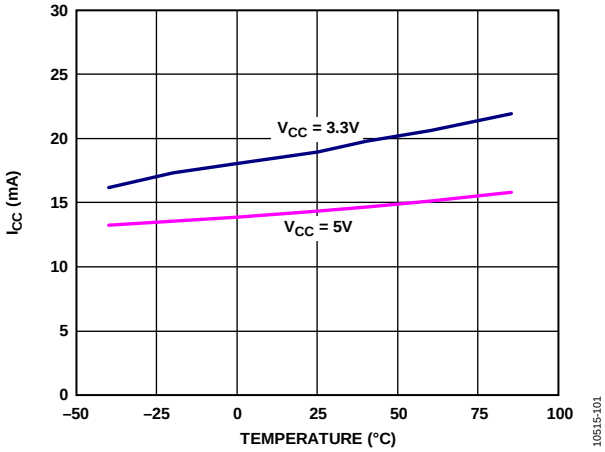



Figure 3. Supply Current vs. Temperature, No Load

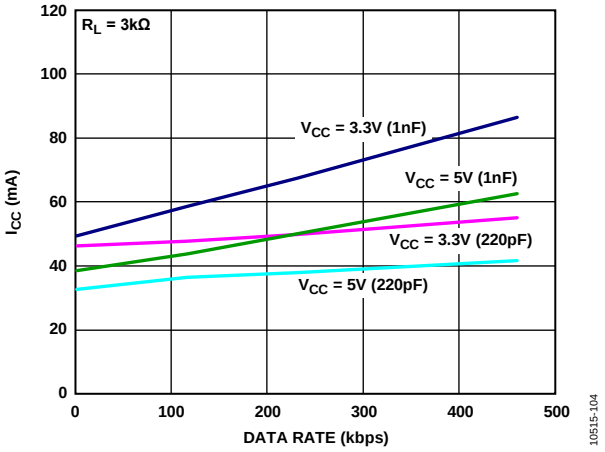



Figure 6. Supply Current vs. Data Rate

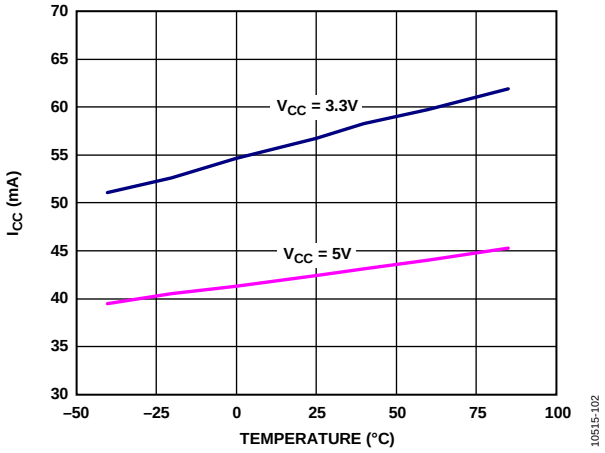



Figure 4. Supply Current vs. Temperature, $R_L$ = 3 kΩ, $C_L$ = 1 nF

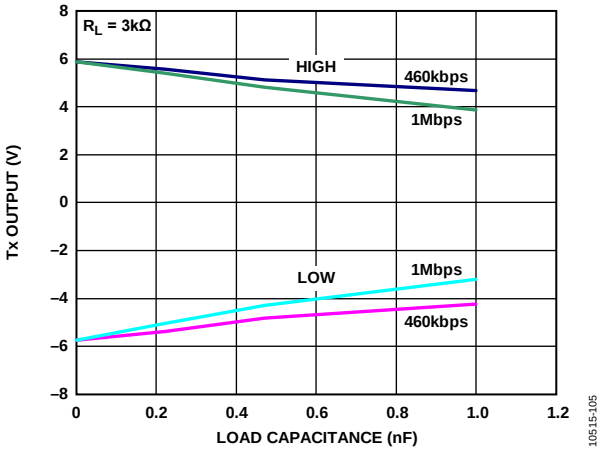



Figure 7. Transmit Output vs. Load Capacitance

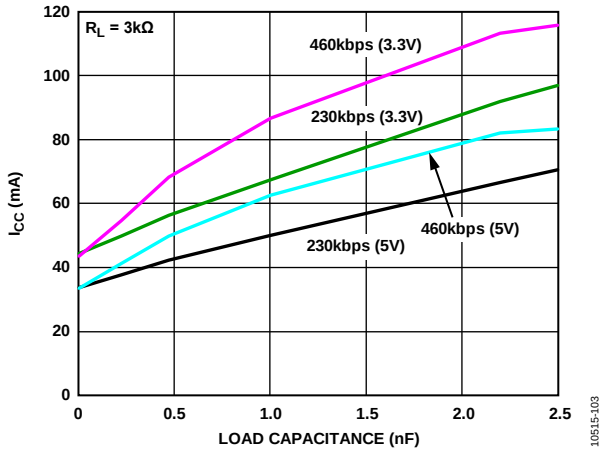



Figure 5. Supply Current vs. Load Capacitance

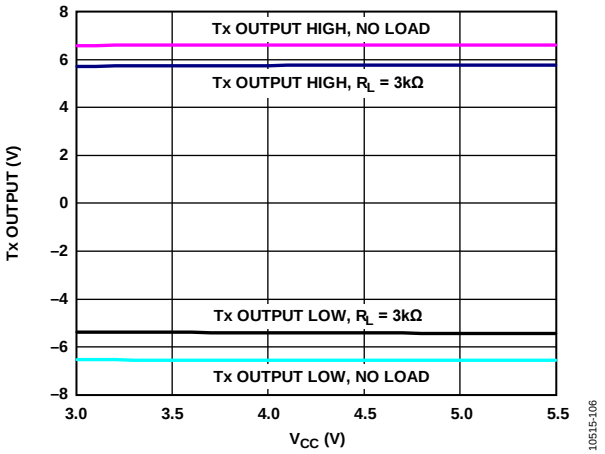



Figure 8. Transmit Output vs. $V_{CC}$

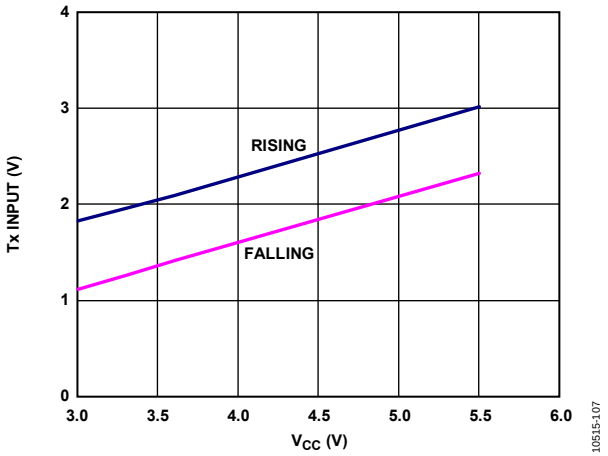



Figure 9. Transmitter Input Threshold vs. $V_{CC}$

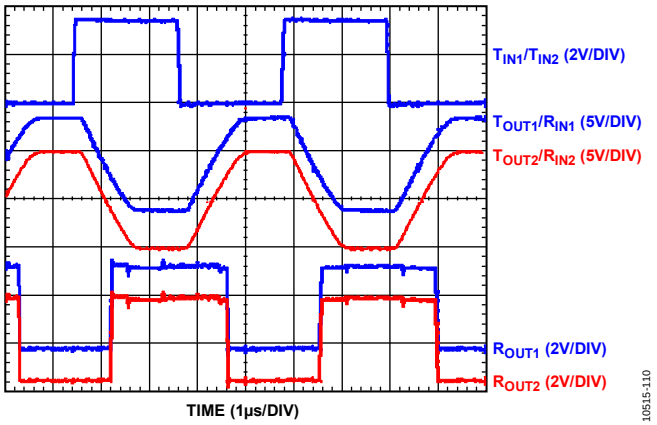



Figure 12. 460 kbps Data Transmission, Driver Outputs Tied to Receiver Inputs

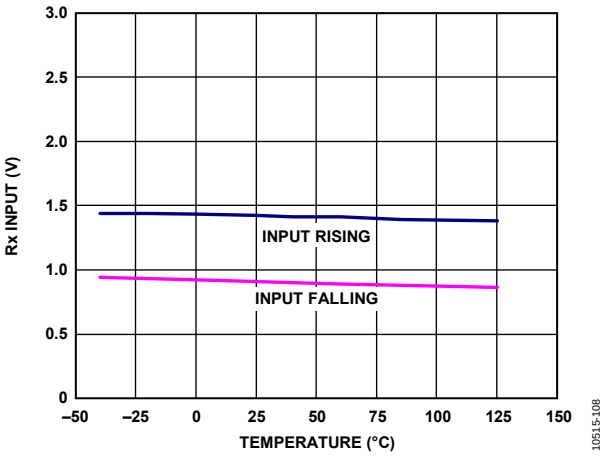



Figure 10. Receiver Input Threshold vs. Temperature

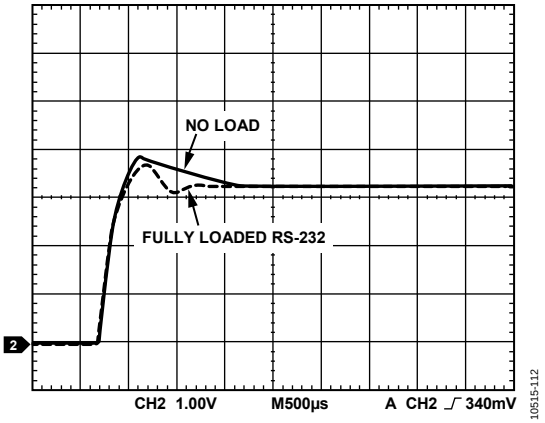



Figure 13. Typical Output Voltage Start-Up Transient, $V_{CC}$ = 3.3 V

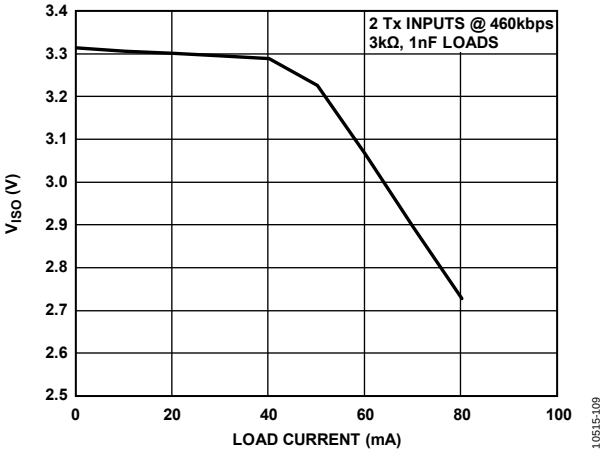



Figure 11. $V_{ISO}$ vs. $V_{ISO}$ Load Current

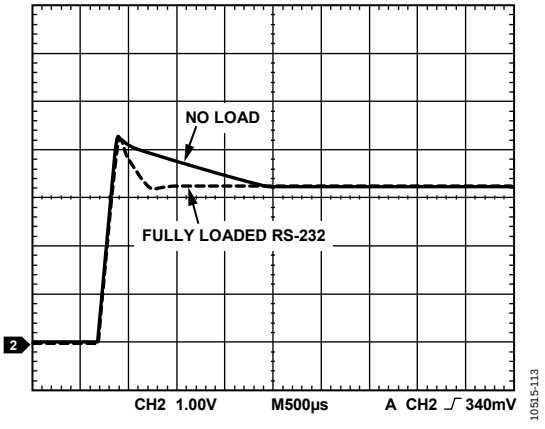



Figure 14. Typical Output Voltage Start-Up Transient, $V_{CC}$ = 5 V

# THEORY OF OPERATION

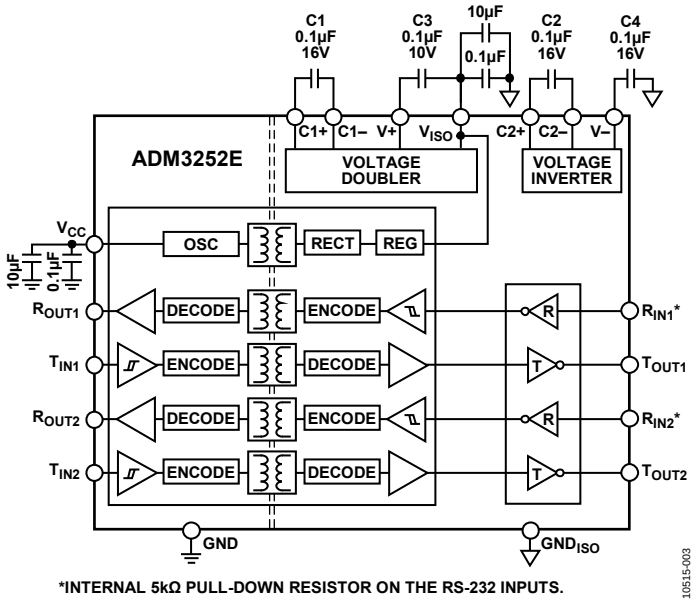



*Figure 15. Functional Block Diagram*

The ADM3252E is a high speed, 2.5 kV, fully isolated, dual-channel RS-232 transceiver device that operates from a single power supply.

The internal circuitry consists of the following main sections:

- Isolation of power and data
- Charge pump voltage converter
- 3.3 V logic to EIA/TIA-232E transmitter
- EIA/TIA-232E to 3.3 V logic receiver

## ISOLATION OF POWER AND DATA

The ADM3252E incorporates a dc-to-dc converter section, which works on principles that are common to most power supply designs. $V_{CC}$ power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power is transferred to the secondary side where it is rectified to a high dc voltage. The power is then linearly regulated to 3.3 V and supplied to the secondary side data section and to the $V_{ISO}$ pin.

Because the oscillator runs at a constant high frequency independent of the load, excess power is internally dissipated in the output voltage regulation process. Limited space for transformer coils and components adds to the internal power dissipation. This results in low power conversion efficiency.

The transmitter input ($T_{INx}$) accepts TTL/CMOS input levels. The driver input signal that is applied to the $T_{INx}$ pins is referenced to logic ground (GND). It is coupled across the isolation barrier, inverted, and then appears at the transceiver section, referenced to isolated ground ($GND_{ISO}$).

Similarly, the receiver input ($R_{INx}$) accepts RS-232 signal levels referenced to isolated ground ($GND_{ISO}$). The $R_{INx}$ input is inverted and coupled across the isolation barrier to appear at the $R_{OUTx}$ pin, referenced to logic ground (GND).

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. Chip scale transformer windings couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer of the winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

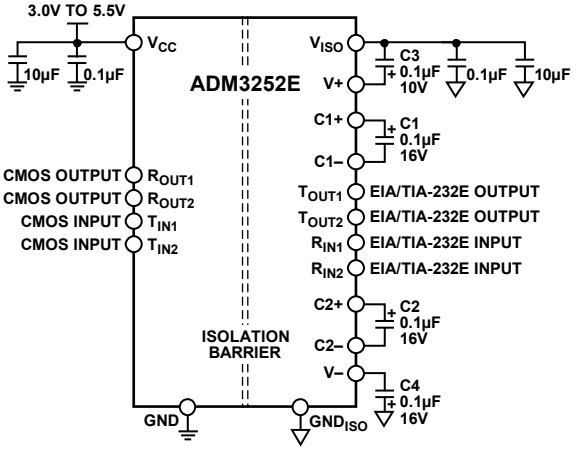



*Figure 16. Typical Operating Circuit*

## CHARGE PUMP VOLTAGE CONVERTER

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±6.6 V supply from the 3.3 V input level. This is achieved in two stages by using a switched capacitor technique, as shown in Figure 17 and Figure 18.

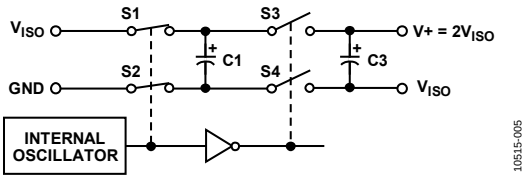



*Figure 17. Charge Pump Voltage Doubler*

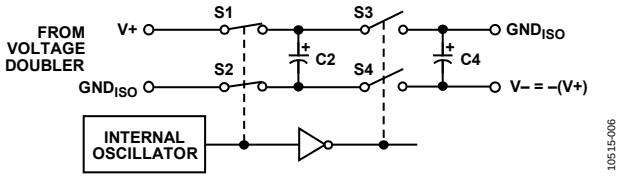



*Figure 18. Charge Pump Voltage Inverter*

In the first stage, the 3.3 V input supply is doubled to 6.6 V using C1 as the charge storage element. In the second stage, the +6.6 V level is inverted to generate −6.6 V using C2 as the storage element. In Figure 17, C3 is connected between V+ and $V_{ISO}$, but it is equally effective if C3 is connected between V+ and $GND_{ISO}$.

Use Capacitor C3 and Capacitor C4 to reduce the output ripple. Their values are not critical and can be increased, if needed. Larger capacitors (up to 10 µF) can be used in place of C1, C2, C3, and C4.

## 3.3 V LOGIC TO EIA/TIA-232E TRANSMITTER

The transmitter driver converts the 3.3 V logic input levels into RS-232 output levels. When driving an RS-232 load with $V_{CC}$ = 3.3 V, the output voltage swing is typically ±6.6 V.

## EIA/TIA-232E TO 3.3 V LOGIC RECEIVER

The receiver is an inverting level shifter that accepts the RS-232 input level and translates it into a 3.3 V logic output level. The input has an internal 5 kΩ pull-down resistor to ground and is protected against overvoltages of up to ±30 V. An unconnected input is pulled to 0 V by the internal 5 kΩ pull-down resistor, resulting in a Logic 1 output level for an unconnected input or for an input connected to GND. The receiver has a Schmitt trigger input with a hysteresis level of 0.1 V. This ensures error free reception for both a noisy input and for an input with slow transition times.

## HIGH BAUD RATE

The ADM3252E offers high slew rates, permitting data transmission at rates well in excess of the EIA/TIA-232E specifications. Higher data rates are possible when running at reduced RS-232 capacitive load levels. A smaller capacitive load, in effect, limits the cable length. See Figure 7 for transmit output voltage levels at 1 Mbps and Figure 19 for a scope plot at 1 Mbps.

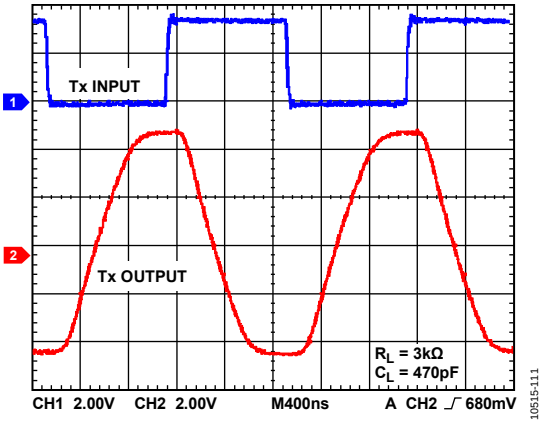



*Figure 19. Scope Plot, 1 Mbps Operation*

# APPLICATIONS INFORMATION

## PCB LAYOUT

The ADM3252E requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 20). Bypass capacitors are conveniently connected between Pin B1 and Pin C1 for $V_{CC}$ and between Pin C10 and Pin D10 for $V_{ISO}$.

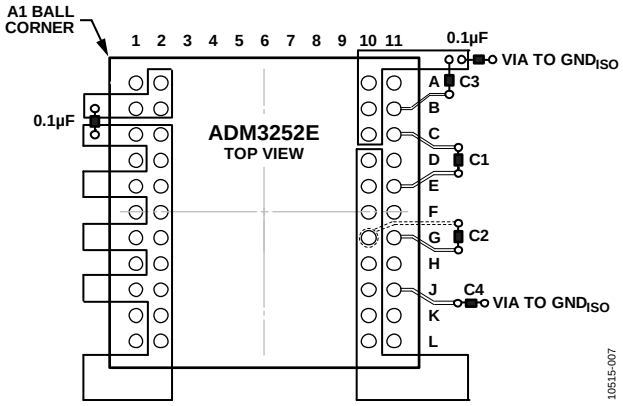



*Figure 20. Recommended Printed Circuit Board Layout*

To suppress noise and reduce ripple, a parallel combination of at least two capacitors is recommended. The recommended capacitor values are 0.1 µF and 10 µF for both $V_{CC}$ and $V_{ISO}$. The smaller capacitor must have a low ESR; best practice suggests use of a ceramic capacitor. Do not exceed 2 mm for the total lead length between both ends of the low ESR capacitor and the input power supply pin.

Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipating into the PCB through the ground pins. If the device is used at high ambient temperatures, take care to provide a thermal path from the ground pins to the PCB ground plane. The board layout in Figure 20 shows enlarged pads for the GND and $GND_{ISO}$ pins. The BGA balls are also grouped together to simplify layout and routing. To significantly reduce the temperature inside the chip, implement multiple vias from each of the pads to the ground plane. The dimensions of the expanded pads are at the discretion of the designer and the available board space.

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side.

The power supply section of the ADM3252E uses a 180 MHz oscillator frequency to pass power through its chip scale transformers. Operation at these high frequencies may raise concerns about radiated emissions and conducted noise. PCB layout and construction are very important tools for controlling radiated emissions. Refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*, for extensive guidance on radiation mechanisms and board layout considerations.

## START-UP BEHAVIOR

The ADM3252E does not contain a soft start circuit. Therefore, the start-up current and voltage behavior must be taken into account when designing with this device.

When power is applied to $V_{CC}$, the input switching circuit begins to operate and draw current when the UVLO minimum voltage is reached (approximately 2.7 V). The switching circuit drives the maximum available power to the output until it reaches the regulation voltage, which is where PWM control begins. The amount of current and the time required to reach regulation voltage depends on the load and the $V_{CC}$ slew rate.

With a fast $V_{CC}$ slew rate (200 µs or less), the peak current draws up to 100 mA/V of $V_{CC}$. The input voltage goes high faster than the output can turn on; therefore, the peak current is proportional to the maximum input voltage.

With a slow $V_{CC}$ slew rate (in the millisecond range), the input voltage is not changing quickly when $V_{CC}$ reaches the UVLO minimum voltage. The current surge is approximately 300 mA because $V_{CC}$ is nearly constant at the 2.7 V UVLO voltage. The behavior during startup is similar to when the device load is a short circuit.

When powering up the device, do not limit the current available to the $V_{CC}$ power pin to less than 300 mA. The ADM3252E device may not be able to drive the output to the regulation point if a current limiting device clamps the $V_{CC}$ voltage during startup. As a result, the ADM3252E device can draw large amounts of current at low voltage for extended periods of time.

The output voltage of the ADM3252E device exhibits $V_{ISO}$ overshoot to approximately 4 V during startup (see Figure 13 and Figure 14). If this overshoot could potentially damage components attached to $V_{ISO}$, a voltage limiting device, such as a Zener diode, can be used to clamp the voltage.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions.

In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses (indicative of the correct input state) are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit. This situation should occur in the ADM3252E during power-up and power-down operations only.

The limitation on the ADM3252E magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
$\beta$ is the magnetic flux density (gauss).
$N$ is the number of turns in the receiving coil.
$r_n$ is the radius of the n$^{th}$ turn in the receiving coil (cm).

Given the geometry of the receiving coil internally and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 21.

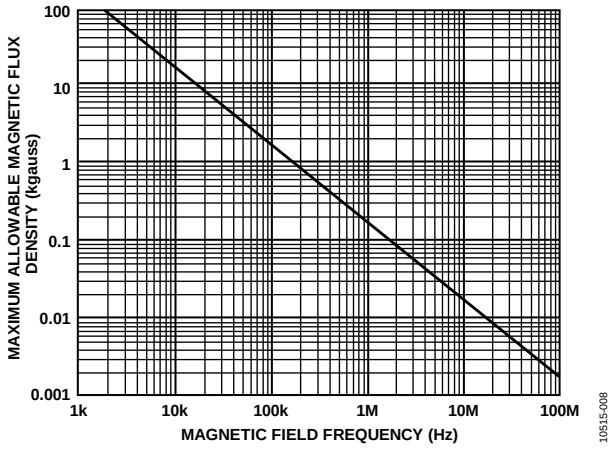



*Figure 21. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the transformers. Figure 22 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 22, the ADM3252E is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current placed 5 mm away from the ADM3252E is required to affect the operation of the component.

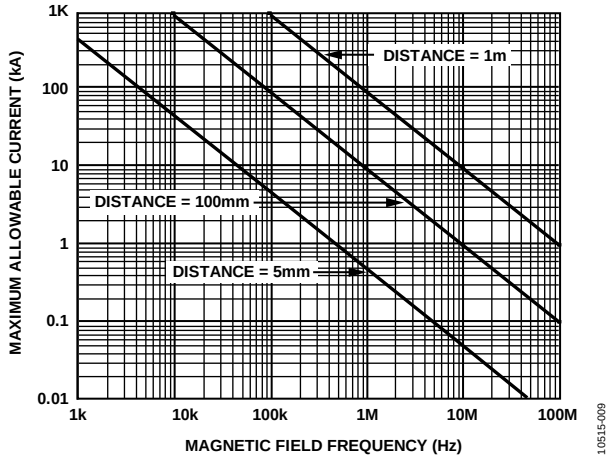



*Figure 22. Maximum Allowable Current for Various Current-to-ADM3252E Spacings*

Note that in the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

## POWER CONSIDERATIONS

The ADM3252E power input, data input channels on the primary side, and data channels on the secondary side are all protected from premature operation by undervoltage lockout (UVLO) circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive and all input channel drivers and refresh circuits are idle. Outputs remain in a high impedance state to prevent transmission of undefined states during power-up and power-down operations.

During the application of power to $V_{CC}$, the primary side circuitry (logic side) is held idle until the UVLO preset voltage is reached. At that time, the data channels are initialized to their default low output states until they receive data pulses from the secondary side (RS-232 side).

When the primary side is above the UVLO threshold, the data input channels sample their inputs and begin sending encoded pulses to the inactive secondary output channels. The outputs on the primary side remain in the default low state because no data comes from the secondary side inputs until secondary side power is established. The primary side oscillator also begins to operate, transferring power to the secondary power circuits.

The secondary $V_{ISO}$ voltage is below its UVLO limit at this point, and the secondary side is not generating a regulation control signal. The primary side power oscillator can free run under these conditions, supplying the maximum amount of power to the secondary side.

As the secondary side voltage rises to its regulation setpoint, a large inrush current transient is present at $V_{CC}$. Upon reaching the regulation point, the regulation control circuit produces the regulation control signal that modulates the oscillator on the primary side. The $V_{CC}$ current is then reduced and it is proportional to the load current. The duration of the inrush current depends on the $V_{ISO}$ loading conditions and on the current and voltage available at the $V_{CC}$ pin.

As the secondary side converter begins to accept power from the primary side, the $V_{ISO}$ voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data is received from the corresponding primary side input. It can take up to 1 µs after the secondary side is initialized for the state of the output to correlate to the primary side input.

Secondary side inputs sample their states and transmit them to the primary side. Outputs are valid about 1 µs after the secondary side becomes active.

Because the rate of charge on the secondary side power supply is dependent on three factors: loading conditions, the input voltage, and the selected output voltage level, take care that the design allows the converter sufficient time to stabilize before valid data is required.

When power is removed from $V_{CC}$, the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge.

The outputs on the secondary side hold the last state that they received from the primary side. Either the UVLO level is reached and the outputs are placed in their high impedance state, or the outputs detect a lack of activity from the primary side inputs and the outputs are set to their default low value before the secondary power reaches UVLO.

## THERMAL ANALYSIS

The ADM3252E device consists of five internal die attached to a PCB laminate. For the purposes of thermal analysis, the device is treated as a thermal unit with the highest junction temperature reflected in the $\theta_{JA}$ value from Table 2. By following the recommendations in the PCB Layout section, thermal resistance to the PCB decreases, thereby allowing increased thermal margin at high ambient temperatures.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3252E.

The insulation lifetime of the ADM3252E depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 23, Figure 24, and Figure 25 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower.

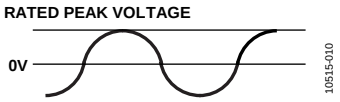



*Figure 23. Bipolar AC Waveform*

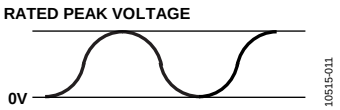



*Figure 24. Unipolar AC Waveform*

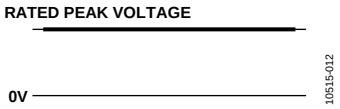
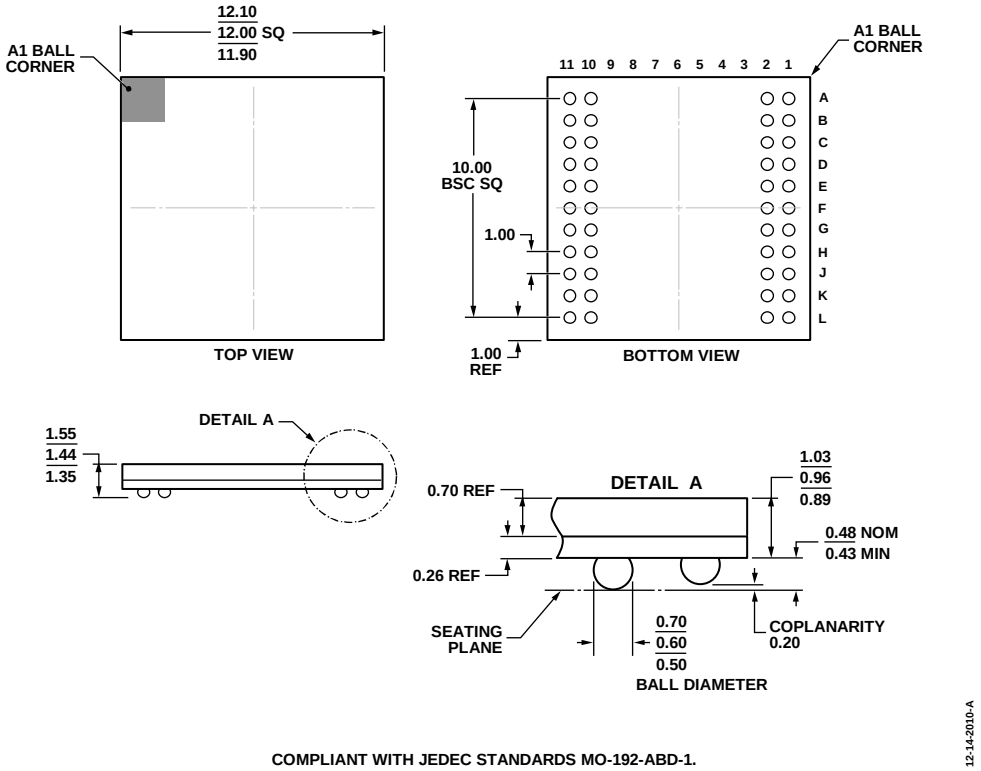



*Figure 25. DC Waveform*

# PACKAGING AND ORDERING INFORMATION

## OUTLINE DIMENSIONS




COMPLIANT WITH JEDEC STANDARDS MO-192-ABD-1.

*Figure 26. 44-Ball Chip Scale Package Ball Grid Array [CSP_BGA]*
*(BC-44-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADM3252EABCZ | −40°C to +85°C | 44-Ball CSP_BGA | BC-44-1 |
| EVAL-ADM3252EEBZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

# NOTES


D10515-0-1/13(A)

# Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

EVAL-ADM3252EEBZ ADM3252EABCZ