

# SN74LVC1G3157 Single-Pole Double-Throw Analog Switch

#### 1 Features

- ESD protection exceeds JESD 22
  - 2000V Human Body Model (A114-A)
  - 1000V Charged-Device Model (C101)
- 1.65V to 5.5V V<sub>CC</sub> operation
- Qualified for 125°C operation
- Specified break-before-make switching
- Rail-to-rail signal handling
- Operating frequency typically 340MHz at room temperature
- High speed, typically 0.5ns ( $V_{CC} = 3V$ ,  $C_L = 50pF$ )
- Low ON-state resistance, typically approximately  $6\Omega (V_{CC} = 4.5V)$
- Latch-up performance exceeds 100mA Per JESD 78, class II

## 2 Applications

- Wearables and mobile devices
- Portable computing
- Internet of things (IoT)
- Audio signal routing
- Remote radio unit
- Portable medical equipment
- Surveillance
- Home automation
- I2C/SPI/UART bus multiplexing
- Wireless charging

## 3 Description

This single channel single-pole double-throw (SPDT) analog switch is designed for 1.65V to 5.5V V<sub>CC</sub> operation.

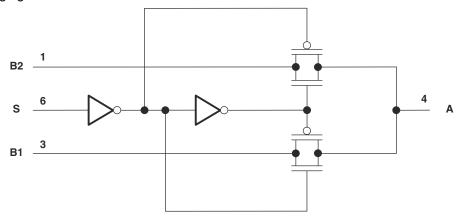
The SN74LVC1G3157 device handles both analog and digital signals. The SN74LVC1G3157 device allows signals with amplitudes of up to V<sub>CC</sub> (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### **Package Information**

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
SN74LVC1G3157	SON (DRY) (6)	1.45mm × 1.00mm
	DSBGA (YZP) (6)	1.41mm × 0.91mm
	SON (DSF) (6)	1.00mm × 1.00mm
	X2SON (DTB) (6)	0.80mm × 1.00mm

For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic** 



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# **4 Pin Configuration and Functions**

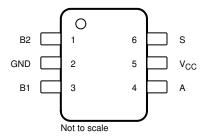


Figure 4-1. DBV Package, 6-Pin SOT-23 (Top View)

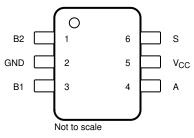


Figure 4-2. DCK Package, 6-Pin SC70 (Top View)

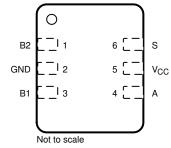


Figure 4-3. DRY Package, 6-Pin SON (Top View)

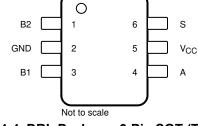


Figure 4-4. DRL Package, 6-Pin SOT (Top View)

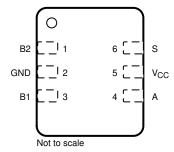


Figure 4-5. DSF Package, 6-Pin SON (Top View)

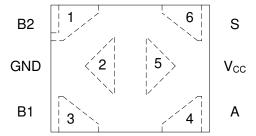


Figure 4-6. DTB Package, 6-Pin X2SON (Top View)

**Table 4-1. Pin Functions** 

	PIN		
NAME	SOT-23, SC70, SON, X2SON, or SOT	TYPE <sup>(1)</sup>	DESCRIPTION
B2	1	I/O	Switch I/O. Set S high to enable.
GND	2	Р	Ground
B1	3	I/O	Switch I/O. Set S low to enable.
A	4	I/O	Common terminal
V <sub>CC</sub>	5	Р	Power supply
S	6	I	Select

(1) I = input, O = output, P = power



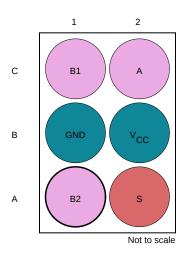


Figure 4-7. YZP Package, 6-Pin DSBGA (Bottom View)



**Table 4-2. Pin Functions** 

	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME	ITPE\''	DESCRIPTION
A1	B2	I/O	Switch I/O. Set S high to enable.
A2	S	I	Select
B1	GND	Р	Ground
B2	V <sub>CC</sub>	Р	Power supply
C1	B1	I/O	Switch I/O. Set S low to enable.
C2	A	I/O	Common terminal

(1) I = input, O = output, P = power

## 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V <sub>CC</sub>	(YZP, DSF. DTB. DRY, DRL) Supply voltage <sup>(2)</sup>	-0.5	6.5	V
V <sub>CC</sub>	(DBV, DCK) Supply voltage <sup>(2)</sup>	-0.5	6	V
V <sub>IN</sub>	(YZP, DSF. DTB. DRY, DRL) Control input voltage <sup>(2)</sup>	-0.5	6.5	V
V <sub>IN</sub>	(DBV, DCK) Control input voltage <sup>(2) (3)</sup>	-0.5	6	V
V <sub>I/O</sub>	Switch I/O voltage <sup>(2) (3) (4) (5)</sup>	-0.5	V <sub>CC</sub> + 0.5V	V
I <sub>IK</sub>	Control input clamp current V <sub>IN</sub> < 0	-50		mA
I <sub>I/OK</sub>	I/O port diode current $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$	-50	50	mA
I <sub>I/O</sub>	On-state switch current <sup>(6)</sup> V <sub>I/O</sub> = 0 to V <sub>CC</sub>	-128	128	mA
	Continuous current through V <sub>CC</sub> or GND	-100	100	mA
TJ	Junction temperature		150	С
T <sub>stg</sub>	Storage temperature	-65	150	С

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5)  $V_1$ ,  $V_0$ ,  $V_A$ , and  $V_{Bn}$  are used to denote specific conditions for  $V_{I/O}$ .
- (6)  $I_{I}$ ,  $I_{O}$ ,  $I_{A}$ , and  $I_{Bn}$  are used to denote specific conditions for  $I_{I/O}$ .



### **5.2 Thermal Information**

			SN74LV	C1G3157				
	THERMAL METRIC	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)	UNIT
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	258.2	286.4	244.1	284.2	324.5	129.4	°C/W
R <sub>θ</sub> JC(top)	Junction-to-case (top) thermal resistance	182.8	224.6	112.5	138.6	150.5	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142.8	143.7	109.9	170.9	239.0	40.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	118.4	124.5	9.3	13.7	17.2	0.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	142.2	142.8	109.3	167.9	238.3	40.2	°C/W

## 5.3 ESD Ratings

				VALUE	UNIT
_ , , , , , , , ,	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±2000	V	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JED specification JESD22-C101 <sup>(2)</sup>	DEC	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufaturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufaturing with a standard ESD control process.

## **5.4 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM MAX	UNIT	
V <sub>CC</sub>	Supply voltage		1.65	5.5	V	
V <sub>I/O</sub>	Switch input or output voltage (Max of V <sub>CC</sub> )		0	V <sub>CC</sub>	V	
V <sub>IN</sub>	Control input voltage		0	5.5	V	
V	High-level input voltage, control	V <sub>CC</sub> = 1.65V to 1.95V	V <sub>CC</sub> * 0.75		V	
V <sub>IH</sub>	input	V <sub>CC</sub> = 2.3V to 5.5V	V <sub>CC</sub> * 0.7		V	
V	Low-level input voltage, control	V <sub>CC</sub> = 1.65V to 1.95V		V <sub>CC</sub> * 0.25	V	
V <sub>IL</sub>	input	V <sub>CC</sub> = 2.3V to 5.5V		V <sub>CC</sub> * 0.3	V	
		V <sub>CC</sub> = 1.8 ± 0.15V		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 2.5 \pm 0.2V$		20	ns/V	
ΔυΔν	Input transition rise or fall rate	V <sub>CC</sub> = 3.3V ± 0.3V		10	ris/v	
		V <sub>CC</sub> = 5V ± 0.5V		10		
		BGA package (YZP)	-40	85		
T <sub>A</sub>	Operating free-air temperature	All other packages (DBV, DCK, DRL, DRY, DSF)	-40	125	°C	

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004)

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## **5.5 Electrical Characteristics**

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	PARAMETER		TEST C	ONDITIONS		MIN	TYP	MAX	UNIT
SN74L\	/C1G3157								
		V <sub>cc</sub> V	V <sub>I/o</sub> V	I <sub>O</sub> mA	T <sub>A</sub>				
					25°C		11		
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 4 mA	-40°C to +85°C			20	
					-40°C to +125°C			20	
		1.65			25°C		15		
			V <sub>I</sub> = 1.65	I <sub>O</sub> = -4 mA	-40°C to +85°C			50	
					-40°C to +125°C			50	
					25°C		8		
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 8 mA	-40°C to +85°C			12	
					-40°C to +125°C			12	
		2.3			25°C		11		
			V <sub>I</sub> = 2.3 V	I <sub>O</sub> = -8 mA	-40°C to +85°C			30	
					-40°C to +125°C			30	
					25°C		7		
r <sub>ON</sub>	ON-state switch resistance <sup>(2)</sup>		V <sub>I</sub> = 0 V	I <sub>O</sub> = 24 mA	-40°C to +85°C			9	Ω
					-40°C to +125°C			9	
		3			25°C		9		
			V <sub>I</sub> = 3 V	I <sub>O</sub> = -24 mA	-40°C to +85°C			20	
				-40°C to +125°C			20		
					25°C		6		-
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 30 mA	-40°C to +85°C			7	
					-40°C to +125°C			7	
				I <sub>O</sub> = 30 mA	25°C		7		
		4.5	V <sub>I</sub> = 2.4 V		-40°C to +85°C			12	
					-40°C to +125°C			12	
					25°C		7		
			V <sub>I</sub> = 4.5 V	I <sub>O</sub> = -30 mA	-40°C to +85°C			15	
					-40°C to +125°C			15	
					25°C			140	
		1.65		I <sub>A</sub> = -4 mA	-40°C to +85°C			140	
					-40°C to +125°C			140	
					25°C			45	
		2.3		I <sub>A</sub> = -8 mA	-40°C to +85°C			45	
	(YZP, DSF. DTB. DRY, DRL)				-40°C to +125°C			45	Ω
r <sub>range</sub>	ON-state switch resistance over signal range <sup>(2)</sup> (3)		$0 \le V_{Bn} \le V_{CC}$		25°C			18	
		3		I <sub>A</sub> = -24 mA	-40°C to +85°C			18	
					-40°C to +125°C			18	
		4.5			25°C			10	
			I <sub>A</sub> = -30 mA	-40°C to +85°C			10	-	
					-40°C to +125°C			10	



Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	PARAMETER		TEST C	ONDITIONS		MIN TYP	MAX	UNIT	
					25°C		200		
		1.65		I <sub>A</sub> = -4 mA	-40°C to +85°C		200		
					-40°C to +125°C		200		
					25°C		65		
		2.3		I <sub>A</sub> = -8 mA	-40°C to +85°C		65		
	(DBV, DCK) ON-state switch		0.414.414		-40°C to +125°C		65	•	
r <sub>range</sub>	resistance over signal range <sup>(2) (3)</sup>		$0 \le V_{Bn} \le V_{CC}$		25°C		25	Ω	
		3		I <sub>A</sub> = -24 mA	-40°C to +85°C		25		
					-40°C to +125°C		25		
					25°C		15		
		4.5		I <sub>A</sub> = -30 mA	-40°C to +85°C		15		
					-40°C to +125°C		15		
					25°C	0.5			
		1.65	V <sub>Bn</sub> = 1.15 V	I <sub>A</sub> = -4 mA	–40°C to +85°C	0.5			
					-40°C to +125°C	0.5			
Maximum ON resistance between any two channels (2) (4) (5)				25°C	0.1				
		2.3	V <sub>Bn</sub> = 1.6 V	I <sub>A</sub> = -8 mA	-40°C to +85°C	0.1		Ω	
					-40°C to +125°C	0.3			
	between any two channels				25°C	0.1			
		3	V <sub>Bn</sub> = 2.1 V	I <sub>A</sub> = -24 mA	-40°C to +85°C	0.1			
					-40°C to +125°C	0.3			
			V <sub>Bn</sub> = 3.15 V	I <sub>A</sub> = -30 mA	25°C	0.1			
		4.5			-40°C to +85°C	0.1			
					-40°C to +125°C	0.2			
					25°C	110			
		1.65		I <sub>A</sub> = -4 mA	-40°C to +85°C	110		-	
					-40°C to +125°C	110			
				I <sub>A</sub> = -8 mA	25°C	26			
		2.3			-40°C to +85°C	26			
	ON resistance			A	-40°C to +125°C	40			
on(flat)	flatness <sup>(2)</sup> (4) (6)		$0 \le V_{Bn} \le V_{CC}$		25°C	9		Ω	
		3		I <sub>A</sub> = -24 mA	-40°C to +85°C	9			
				A	-40°C to +125°C	10			
					25°C	4			
		4.5		I <sub>A</sub> = -30 mA	-40°C to +85°C	4			
				,A 00	-40°C to +125°C	5			
					25°C	±0.05	±0.1		
l <sub>off</sub> (7)	Switch OFF leakage current	1.65 to 5.5	$0 \le V_1, V_0 \le V_0$	20	-40°C to +85°C		±1	μA	
OII	owner or r loanago carronic	1.00 to 0.0	0 - 11, 10 - 10		-40°C to +125°C		±1	μ, ι	
					25°C		±0.1		
S(on)	ON-state switch leakage	5.5	$V_I = V_{CC}$ or GN	ID $V_0 = Open$	-40°C to +85°C	·	±1	μA	
S(011)	current	3.5	1, 100 01 01	, • <sub>0</sub> Opon	-40°C to +125°C		±1	۳,,	
					25°C	±0.05	±0.1		
l.s.	Control input current	0 to 5.5 $0 \le V_{IN} \le V_{CC}$			-40°C to +85°C	10.03	±0.1	μΔ	
I <sub>IN</sub>	John of hiput current	0 10 0.0	O = VIN = VCC		-40°C to +65°C		I 1	μA	

Over operating free-air temperature range (unless otherwise noted)(1)

	PARAMETER		TEST CONDITIO	INS	MIN 7	ГΥР	MAX	UNIT
				25°C			1	
I <sub>CC</sub>	Supply current	5.5	S = V <sub>CC</sub> or GND	-40°C to +85°C			10	μΑ
				-40°C to +125°C			35	
	Quiescent Device Current,			25°C			500	
$\Delta I_{CC}$	I <sub>DD</sub> Max	5.5	S = V <sub>CC</sub> - 0.6 V	-40°C to +85°C			500	μΑ
				-40°C to +125°C			500	
				25°C		2.7		
Cı	Control input capacitance	5	5 S (VDD/2)	-40°C to +85°C		2.7		pF
				-40°C to +125°C		2.7		
	Switch input/output			25°C		5.2		
C <sub>io(off)</sub>	capacitance	5	Bn (VDD/2)	-40°C to +85°C		5.2		pF
				-40°C to +125°C		5.2		
				25°C	1	7.3		
			Bn (VDD/2)	-40°C to +85°C	1	7.3		
	Switch input/output	_		-40°C to +125°C	1	7.3		
C <sub>io(on)</sub>	C <sub>io(on)</sub> capacitance			25°C	1	7.3		pF
			A (VDD/2)	-40°C to +85°C	1	7.3		
				-40°C to +125°C	1	7.3		

- (1)
- (2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
- Specified by design
- $\Delta r_{on} = r_{on(max)} r_{on(min)}$  measured at identical  $V_{CC}$ , temperature, and voltage levels This parameter is characterized, but not production tested.
- Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.
- $I_{\text{off}}$  is the same as  $I_{\text{S(off)}}$  (off-state switch leakage current).

## 5.6 Switching Characteristics 85C (DBV, DCK)

 $T_A = -40 \text{ to } +85^{\circ}\text{C}$ 

	Parameter	FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM MAX	UNIT
				1.8 V ± 0.15 V		2	
$t_{pd}$ $R_L = 250\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$	B = 2500 C = 50°F V = V	A or Bn	Bn or A	2.5 V ± 0.2 V		1.2	
	N <sub>C</sub> = 250Ω, C <sub>L</sub> = 30βr, V <sub>load</sub> = V <sub>CC</sub>	A OI BII	BITOTA	3.3 V ± 0.3 V		0.8	ns
				5 V ± 0.5 V		0.3	
				1.8 V ± 0.15 V	5	24	
	B = 2500 C = 50°F V = V			2.5 V ± 0.2 V	3.5	14	
t <sub>en</sub>	$R_L = 250\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$			3.3 V ± 0.3 V	2.5	7.6	
		S	Bn	5 V ± 0.5 V	1.7	5.7	
		5	ы	1.8 V ± 0.15 V	3	13	ns
	$R_L = 250\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$ , $V_{\blacktriangle} =$			2.5 V ± 0.2 V	2	7.5	
	0.3V			3.3 V ± 0.3 V	1.5	6	
				5 V ± 0.5 V	8.0	5	



 $T_A = -40 \text{ to } +85^{\circ}\text{C}$ 

	Parameter	FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM	MAX	UNIT
				1.8 V ± 0.15 V	0.5			
_	Break before make time			2.5 V ± 0.2 V	0.5			20
T <sub>B-M</sub>	Break before make time			3.3 V ± 0.3 V	0.5			ns
				5 V ± 0.5 V	0.5			

# 5.7 Switching Characteristics 125C (DBV, DCK)

 $T_A = -40 \text{ to } +125^{\circ}\text{C}$ 

Parameter		FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM MAX	UNIT
				1.8 V ± 0.15 V		2	
	$R_L = 250\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$	A or Bn	Bn or A	2.5 V ± 0.2 V		1.2	ns
t <sub>pd</sub>	1   2   2   2   2   2   2   2   2   2	A OI BII	BITOTA	3.3 V ± 0.3 V		0.8	113
				5 V ± 0.5 V		0.5	
	$t_{en}$ $R_L = 250\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$			1.8 V ± 0.15 V	1	24.5	
		- S	Bn	2.5 V ± 0.2 V	1	14.5	
<sup>t</sup> en				3.3 V ± 0.3 V	2.5	8	
				5 V ± 0.5 V	1.7	7	
			Ы	1.8 V ± 0.15 V	2.5	13.5	115
	$R_L = 250\Omega$ , $C_L = 50$ pF, $V_{load} = V_{CC}$ , $V_{\blacktriangle} =$			2.5 V ± 0.2 V	2	8	
t <sub>dis</sub>	0.3V			3.3 V ± 0.3 V	1.5	6.5	
				5 V ± 0.5 V	0.8	5	
				1.8 V ± 0.15 V	0.5		
_	Break before make time			2.5 V ± 0.2 V	0.5		no
T <sub>B-M</sub>	Dieak beiole make time			3.3 V ± 0.3 V	0.5		ns
				5 V ± 0.5 V	0.5		

# 5.8 Switching Characteristics 85C (YZP, DSF. DTB. DRY, DRL)

 $T_A = -40 \text{ to } +85^{\circ}\text{C}$ 

Parameter		FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM I	MAX	UNIT
				1.8 V ± 0.15 V			2	
<b>t</b> .	$R_L = 500\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$	A or Bn	Bn or A	2.5 V ± 0.2 V			1.2	ne
t <sub>pd</sub>	N <sub>L</sub> = 300Ω, O <sub>L</sub> = 30βΓ, V <sub>load</sub> = V <sub>CC</sub>	A OI BII		3.3 V ± 0.3 V			8.0	ns
				5 V ± 0.5 V			0.3	
	$R_L = 500\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$			1.8 V ± 0.15 V	7		24	
				2.5 V ± 0.2 V	3.5		14	
t <sub>en</sub>				3.3 V ± 0.3 V	2.5		7.6	
		S		5 V ± 0.5 V	1.7		5.7	no
		3	Bn	1.8 V ± 0.15 V	3	-	13	ns
	$R_L = 500\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$ , $V_{\Delta} =$			2.5 V ± 0.2 V	2		7.5	
t <sub>dis</sub>	0.3V			3.3 V ± 0.3 V	1.5		5.3	
				5 V ± 0.5 V	8.0		3.8	

 $T_A = -40 \text{ to } +85^{\circ}\text{C}$ 

	Parameter	FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM	MAX	UNIT
				1.8 V ± 0.15 V	0.5			
_	Donald harfara was har firm			2.5 V ± 0.2 V	0.5			20
T <sub>B-M</sub>	Break before make time			3.3 V ± 0.3 V	0.5			ns
				5 V ± 0.5 V	0.5			

## 5.9 Switching Characteristics 125C (YZP, DSF. DTB. DRY, DRL)

 $T_A = -40 \text{ to } +125^{\circ}\text{C}$ 

	Parameter	FROM (INPUT)	то (оитрит)	V <sub>cc</sub>	MIN	NOM MAX	UNIT
				1.8 V ± 0.15 V		2	
	$R_L = 500\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$	A or Bn	Bn or A	2.5 V ± 0.2 V		1.2	ns
t <sub>pd</sub>	1   1   20022, OL	A OI BII	BITOLA	3.3 V ± 0.3 V		0.8	113
				5 V ± 0.5 V		0.5	
	$R_L = 500\Omega$ , $C_L = 50pF$ , $V_{load} = V_{CC}$			1.8 V ± 0.15 V	1	24.5	
t <sub>en</sub>		- S	Bn	2.5 V ± 0.2 V	1	14.5	
				3.3 V ± 0.3 V	2.5	8	
				5 V ± 0.5 V	1.7	6	
			Ы	1.8 V ± 0.15 V	2.5	13.5	ns
	$R_L$ = 500 $\Omega$ , $C_L$ = 50pF, $V_{load}$ = $V_{CC}$ , $V_{\Delta}$ =			2.5 V ± 0.2 V	2	8	
t <sub>dis</sub>	0.3V			3.3 V ± 0.3 V	1.5	5.5	
				5 V ± 0.5 V	8.0	4	
				1.8 V ± 0.15 V	0.5		
_	Brook hoforo make time			2.5 V ± 0.2 V	0.5		no
T <sub>B-M</sub>	Break before make time			3.3 V ± 0.3 V	0.5		ns
				5 V ± 0.5 V	0.5		

## **5.10 Analog Channel Specifications**

over operating free-air temperature range (unless otherwise noted)

Parameter	FROM (INPUT)	то (оитрит)	TEST CONDITIONS	V <sub>cc</sub>	MIN NOM N	AX UNIT	Т
			R <sub>I</sub> = 50 Ω, f <sub>in</sub> =	1.65 V	340		
Frequency response	A or Bn	Bn or A		2.3 V	340	MHz	7
(switch on) <sup>(1)</sup>	A OI BII	BIT OF A	sine wave	3 V	340	1011 12	_
				4.5 V	340		
	B1 or B2			1.65 V	-54		
Crosstalk (between			$R_L = 50 \Omega$ , $f_{in} = 10$ MHz (sine wave)	2.3 V	-54	dB	
switches)(2)				3 V	-54	UB UB	
,				4.5 V	-54		
				1.65 V	-57		
Feed through attenuation		Dn or A	$C_L = 5 \text{ pF, } R_L =$	2.3 V	-57	dB	
(switch off)(2)	A or Bn	Bn or A	$50 \Omega$ , $f_{in} = 10 MHz$ (sine wave)	3 V	-57	UD UD	
,			,	4.5 V	-57		
Charge	S (Va = VDD/2)	^	C <sub>L</sub> = 0.1 nF, R <sub>L</sub> = 1	3.3 V	3		
injection	S (Vs = VDD/2)	A	MΩ	5 V	7	pC	



over operating free-air temperature range (unless otherwise noted)

Parameter	FROM (INPUT)	то (оитрит)	TEST CONDITIONS	V <sub>cc</sub>	MIN NOM	MAX	UNIT
Total harmonic distortion (YZ P, DSF. DTB. DRY, DRL)	A or Bn	Bn or A	$\begin{array}{l} V_{I}=1.4\;V_{p\text{-}p},\;\text{Vbias}\\ =\;\text{Vcc/2},\;R_{L}=\\ 10\text{k}\Omega,\;f_{in}=600\\ \text{Hz}\;\text{to}\;20\text{kHz}\;\text{(sine}\\ \text{wave)} \end{array}$	1.65 V	0.1		%
Total harmonic distortion (DBV, DCK)	A or Bn	Bn or A	$\begin{array}{l} V_{l}=1.4\ V_{p\text{-}p},\ \text{Vbias}\\ =\ \text{Vcc/2},\ R_{L}=\\ 10k\Omega,\ f_{in}=600\\ \text{Hz to 20kHz (sine}\\ \text{wave)} \end{array}$	1.65 V	0.5		%
			V <sub>I</sub> = 2.0 V <sub>p-p</sub> , Vbias	2.3 V	0.025		
Total harmonic	A or Bn	Bn or A	= Vcc/2, R <sub>L</sub> = 10kΩ, f <sub>in</sub> = 600	3 V	0.015		%
distortion	A OI DII	DIT OF A	Hz to 20kHz (sine wave)	4.5 V	0.01		, •

<sup>(1)</sup> Set fin to 0 dBm and provide a bias of 0.4 V. Increase fin frequency until the gain is 3 dB below the insertion loss.

<sup>(2)</sup> Set fin to 0 dBm and provide a bias of 0.4 V.



## **6 Parameter Measurement Information**

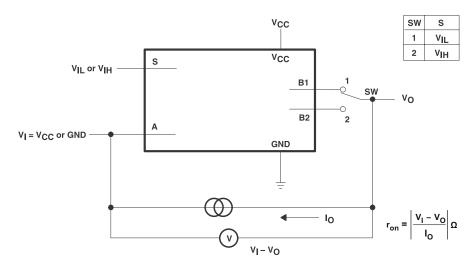
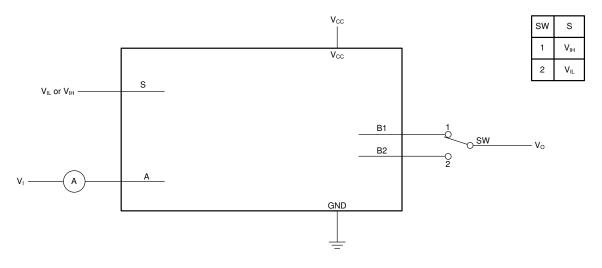


Figure 6-1. ON-State Resistance Test Circuit



 $\begin{aligned} & \text{Condition 1: } V_{I} = GND, \ V_{O} = V_{CC} \\ & \text{Condition 2: } V_{I} = V_{CC}, \ V_{O} = GND \end{aligned}$ 

Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

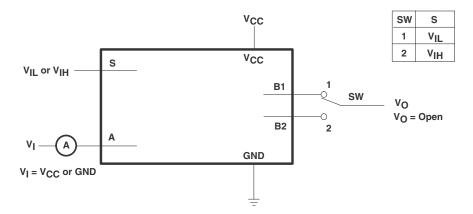
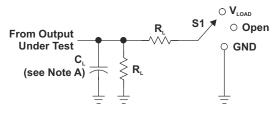


Figure 6-3. ON-State Switch Leakage-Current Test Circuit

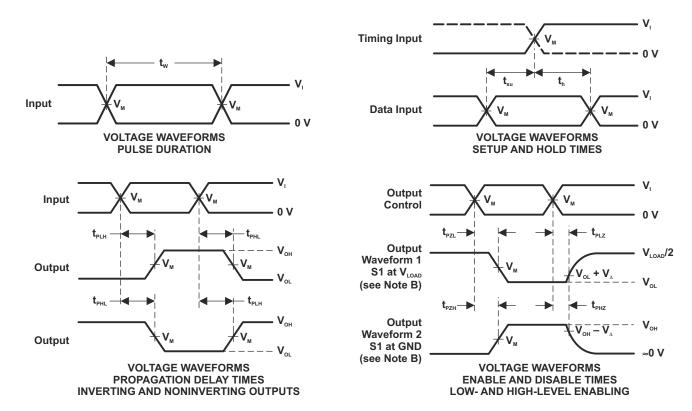




TEST	S1
$t_{_{PLH}}/t_{_{PHL}}$	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

**LOAD CIRCUIT** 

.,	INI	PUTS		.,			.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	R <sub>⊾</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{o}$  = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\mbox{\tiny PLZ}}$  and  $\dot{t}_{\mbox{\tiny PHZ}}$  are the same as  $t_{\mbox{\tiny dis}}.$
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{\mbox{\tiny PLH}}$  and  $t_{\mbox{\tiny PHL}}$  are the same as  $t_{\mbox{\tiny pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Load Circuit and Voltage Waveforms



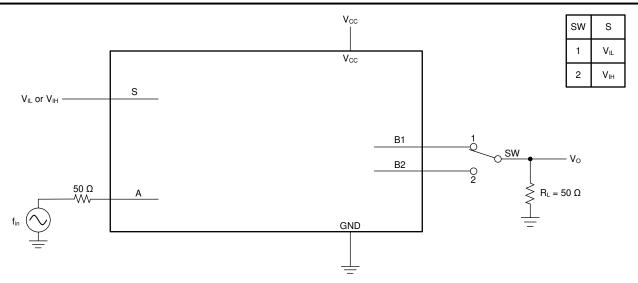


Figure 6-5. Frequency Response (Switch On)

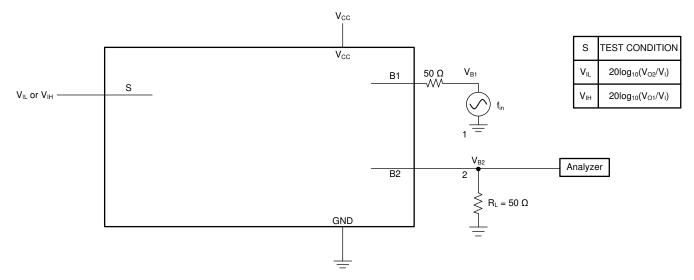


Figure 6-6. Crosstalk (Between Switches)



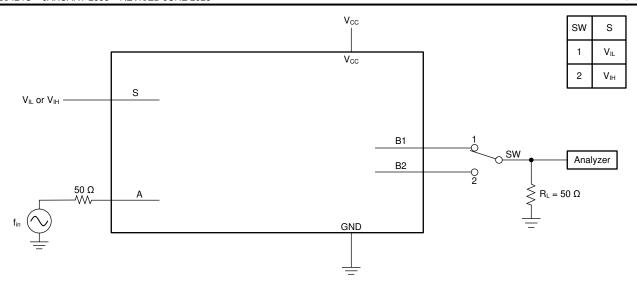


Figure 6-7. Feed Through

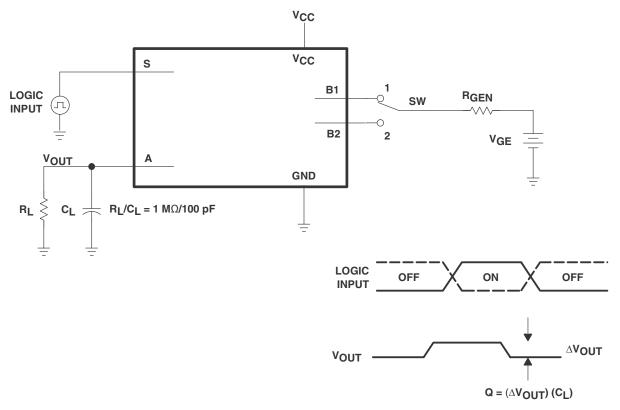


Figure 6-8. Charge-Injection Test



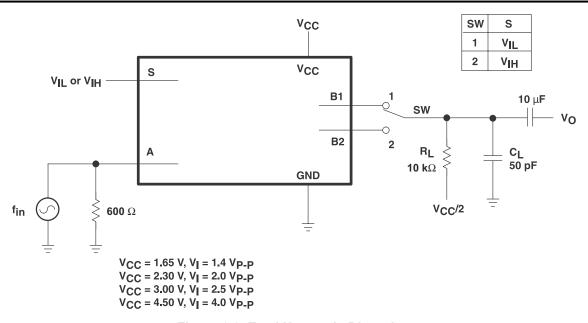


Figure 6-9. Total Harmonic Distortion

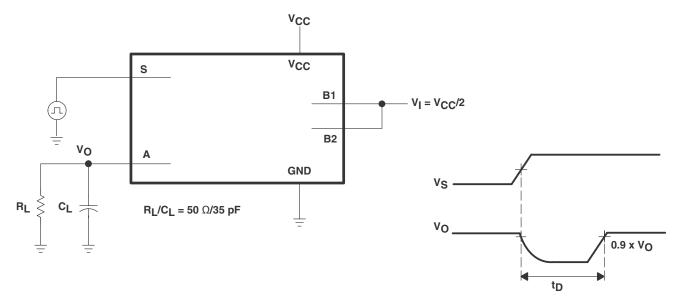


Figure 6-10. Break-Before-Make Internal Timing

## 7 Detailed Description

### 7.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65V to 5.5V  $V_{CC}$  operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to  $V_{CC}$  (peak) to be transmitted in either direction.

## 7.2 Functional Block Diagram

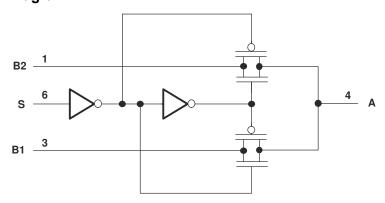


Figure 7-1. Logic Diagram (Positive Logic)

## 7.3 Feature Description

The 1.65V to 5.5V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

### 7.4 Device Functional Modes

Table 7-1 lists the ON channel when one of the control inputs is selected.

**Table 7-1. Function Table** 

CONTROL INPUTS	ON CHANNEL
L	B1
Н	B2

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## 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches.

### 8.2 Typical Application

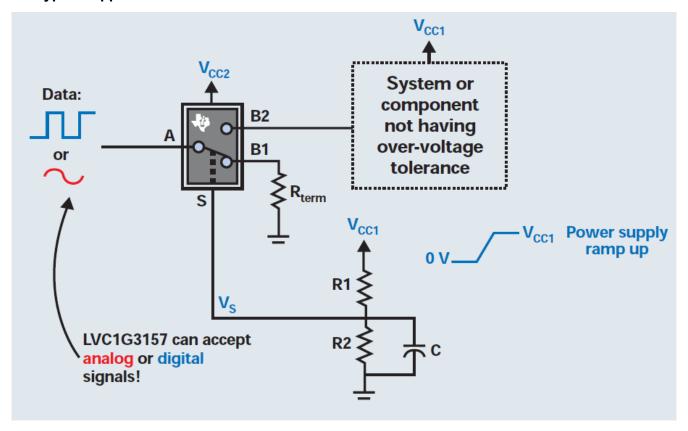


Figure 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until  $V_{CC}$  has ramped to a level in *Section 5.4* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

#### 8.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/ system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0V) to half the supply voltage (VCC1/2).

$$Set\left(\frac{R2}{R1 + R2} \times VCC1 > VIH\right) of the select pin$$
(1)

Choose Rs and C to achieve the desired delay. When  $V_S$  goes high, the signal will be passed.

#### 8.2.3 Application Curve

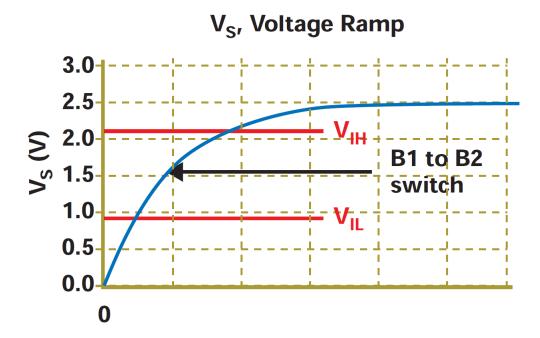


Figure 8-2. V<sub>S</sub> Voltage Ramp

## 9 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the  $V_{CC}$  pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

## 10 Layout

## 10.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either  $50\Omega$  or  $75\Omega$ , as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

### 10.2 Layout Example

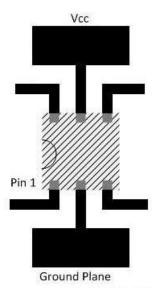


Figure 10-1. Recommended Layout Example



## 11 Device and Documentation Support

## 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Implications of Slow or Floating CMOS Inputs
- Texas Instruments, SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 11.4 Trademarks

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### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

	anges from Revision N (May 2025) to Revision O (June 2025) Separated relevant DBV and DCK specifications from other packages	<b>Page</b> 5
Ch	anges from Revision M (August 2022) to Revision N (May 2025)	Page
•	ABS max supply voltage changed	5
•	Updated thermal parameters for DBV and DCK	6
•	r <sub>range</sub> updated	7
•	Updated enable timing for 85C 1.8V and 125C 5V conditions	9
	Updated disable timing for 85C 5V and 125C 3.3V, 5V conditions	
	Updated THD test conditions and 1.65V specification	

Changes from Revision L (May 2017) to Revision M (August 2022) 

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Page

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Updated the Pin Configuration and Functions section	3
Updated the equation in the Detailed Design Procedure section	
	Page
Deleted Feature "Useful for Both Analog and Digital Applications"	
Deleted Feature "High Degree of Linearity"	
Changed the first sentence of the <i>Description</i> From: "This single-pole double-the company of the company	
channel single pole double-throw (SPDT)"	1
Added the X2SON (DTB) package to the Device Information	
Added the X2SON (DTB) Package, to the Pin Configuration and Functions      Channel Figure 6.0 Frage SW4 = V to SW4 = V Frage SW4 = V to SW4 = V	
<ul> <li>Changed Figure 6-2, From: SW1 = V<sub>IL</sub> to SW1 = V<sub>IH</sub>, From: SW2 = V<sub>IH</sub> to: SW2</li> </ul>	
Changed Figure 6-5  Added a series 50 O resistant on P4 in Figure 6.6	13
Added a series 50-Ω resistor on B1 in Figure 6-6	
Changed Figure 6-7	13
Changes from Revision J (June 2016) to Revision K (January 2017)	Page
Added new applications to Applications section	1
Changes from Revision I (June 2015) to Revision J (June 2016)  Deleted 200V Machine Model (A115-A) from Features	Page
Changed Feature From: "Operating Frequency Typically 300MHz at Room Tem Frequency Typically 340MHz at Room Temperature"	perature" To: "Operating
Updated Device Information table	1
Updated pinout images for all Packages	3
Added Receiving Notification of Documentation Updates section	
Changes from Revision H (May 2012) to Revision I (June 2015)	Page
Added Device Information table, Pin Configuration and Functions section, ESD	
Description section, Device Functional Modes, Application and Implementation	
Recommendations section, Layout section, Device and Documentation Suppor	
Packaging, and Orderable Information section	
Updated Features	
Changes from Revision G (September 2011) to Revision H (May 2012)	Page
Changed YZP with correct pin labels	

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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15-Jul-2025

## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74LVC1G3157DBVR1G4	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DRLRG4	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DRLRG4.B	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DSFRG4	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
74LVC1G3157DSFRG4.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DCK3	Obsolete	Production	SC70 (DCK)   6	-	-	Call TI	Call TI	-40 to 125	C5Z
SN74LVC1G3157DCKR	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5 R)
SN74LVC1G3157DCKR.A	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5 R)
SN74LVC1G3157DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5 R)
SN74LVC1G3157DRLR	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.B	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRY2	Obsolete	Production	SON (DRY)   6	-	-	Call TI	Call TI	-40 to 125	C5
SN74LVC1G3157DRYR	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.A	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG   NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5

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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
						(4)	(5)		
SN74LVC1G3157DSFR.A	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DTBR	Active	Production	X2SON (DTB)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157DTBR.B	Active	Production	X2SON (DTB)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157YZPR	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N
SN74LVC1G3157YZPR.B	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC1G3157:

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## PACKAGE OPTION ADDENDUM

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• Automotive : SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

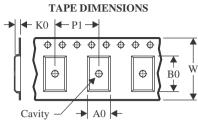
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

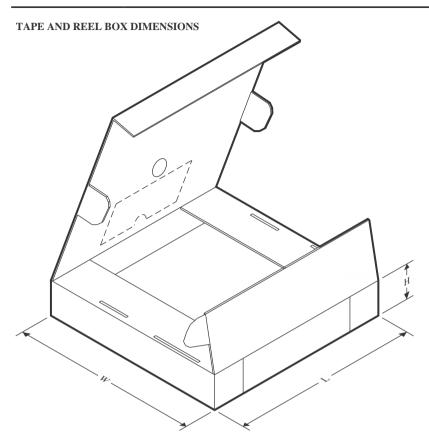


#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
74LVC1G3157DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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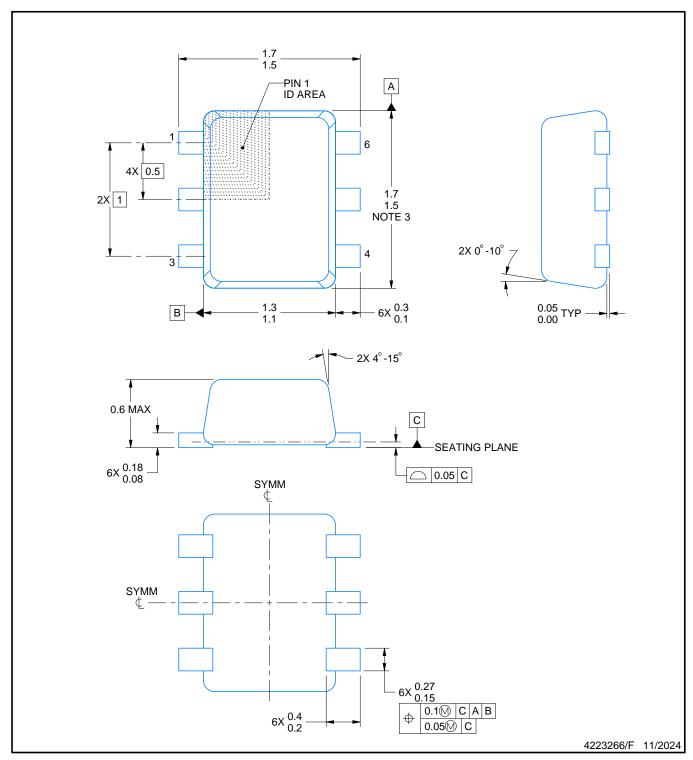


\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	210.0	185.0	35.0
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
74LVC1G3157DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0



PLASTIC SMALL OUTLINE



#### NOTES:

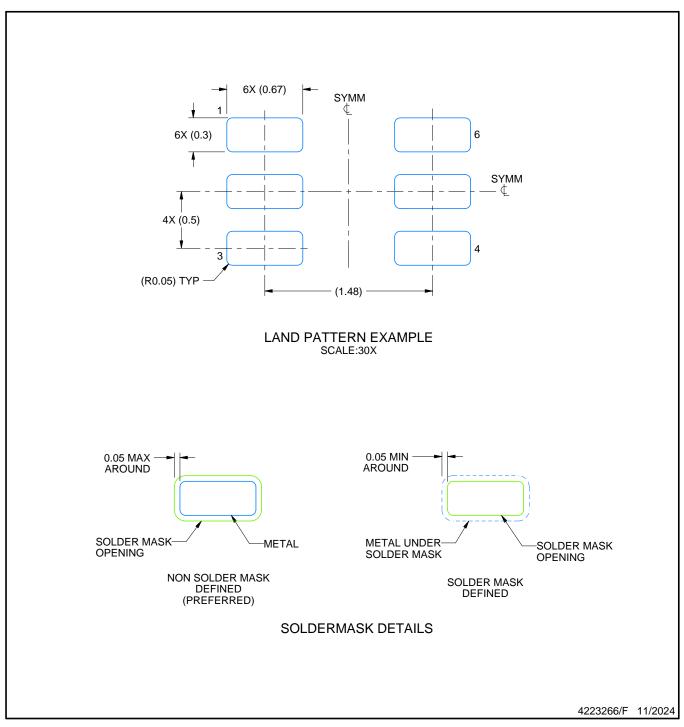
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-293 Variation UAAD



PLASTIC SMALL OUTLINE

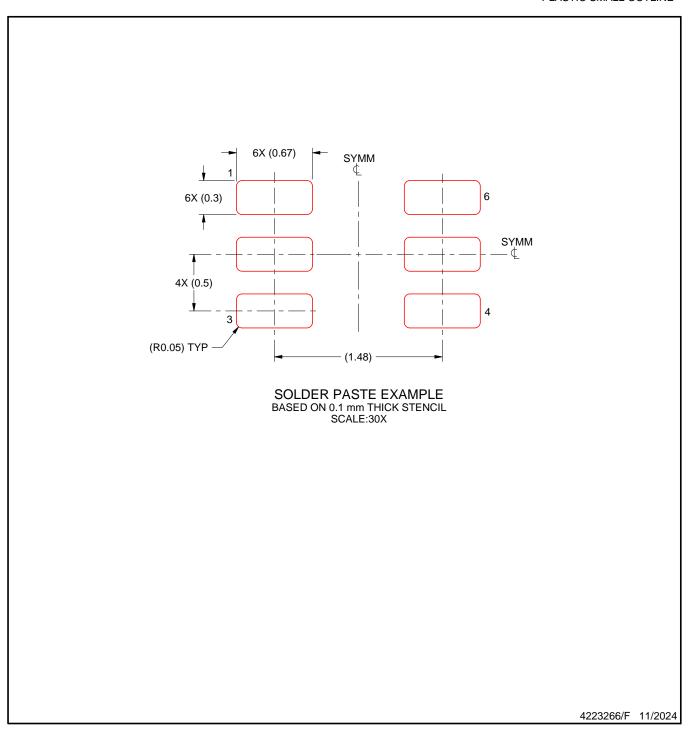


NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



PLASTIC SMALL OUTLINE



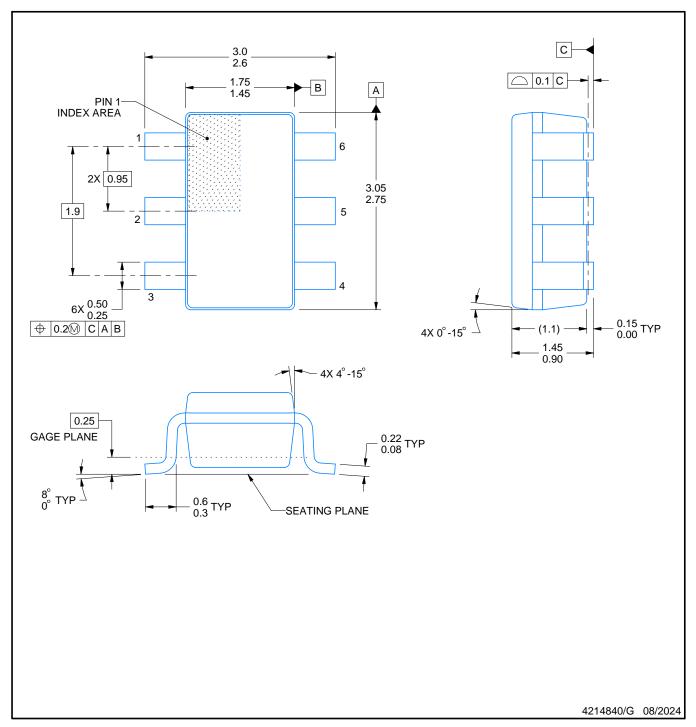
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

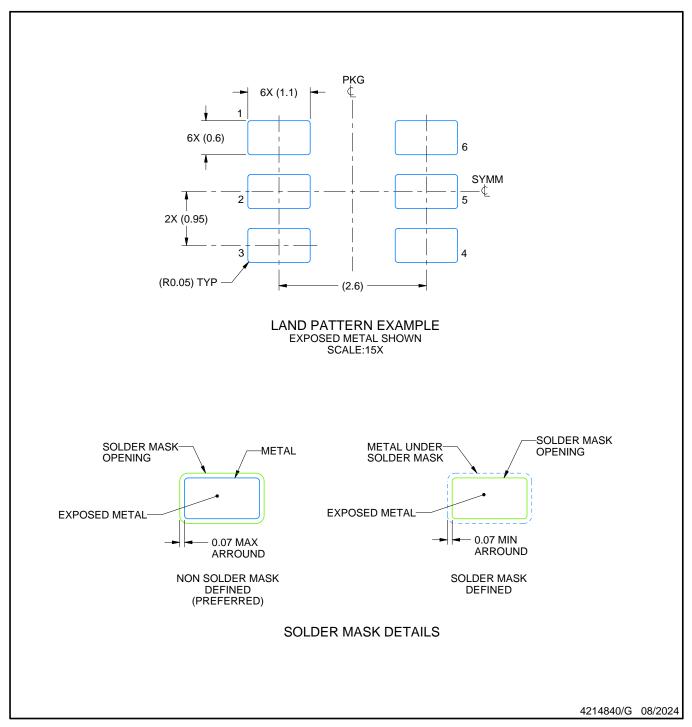
  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.



SMALL OUTLINE TRANSISTOR



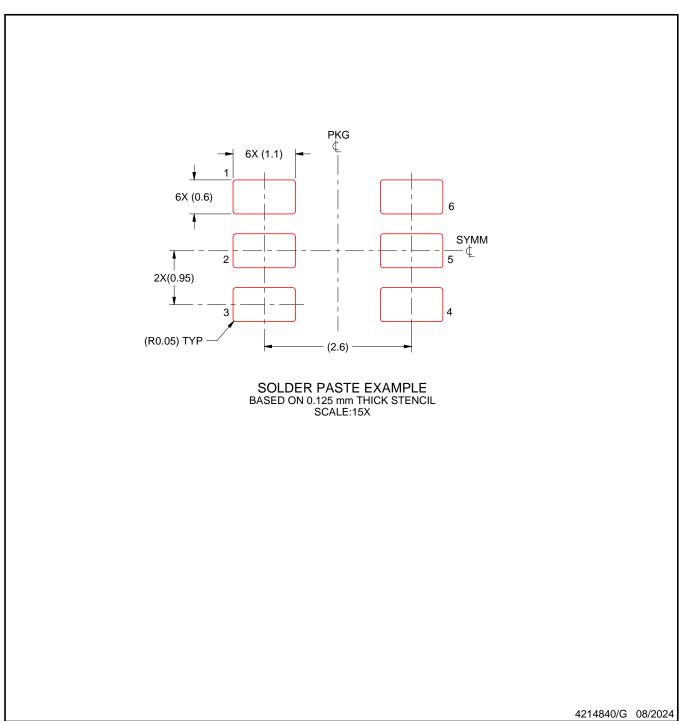
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



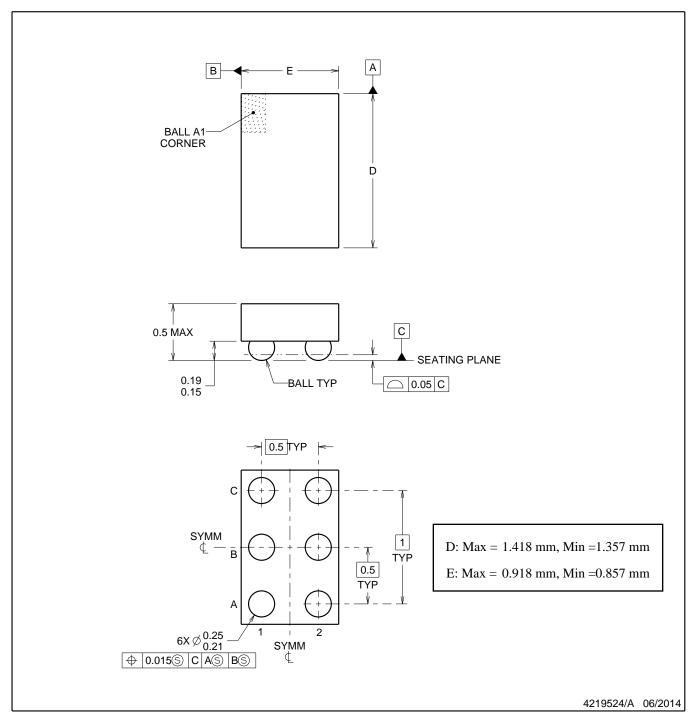
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



#### NOTES:

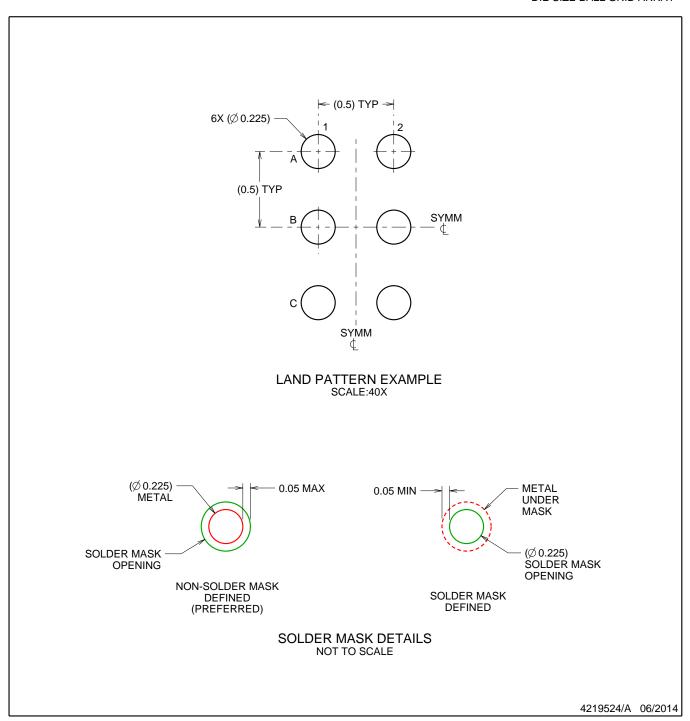
NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. NanoFree<sup>™</sup> package configuration.



DIE SIZE BALL GRID ARRAY

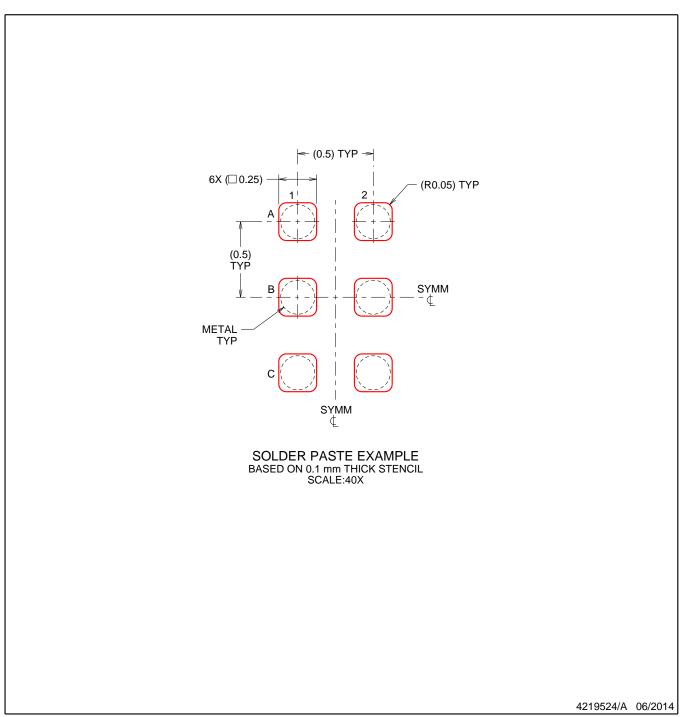


NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



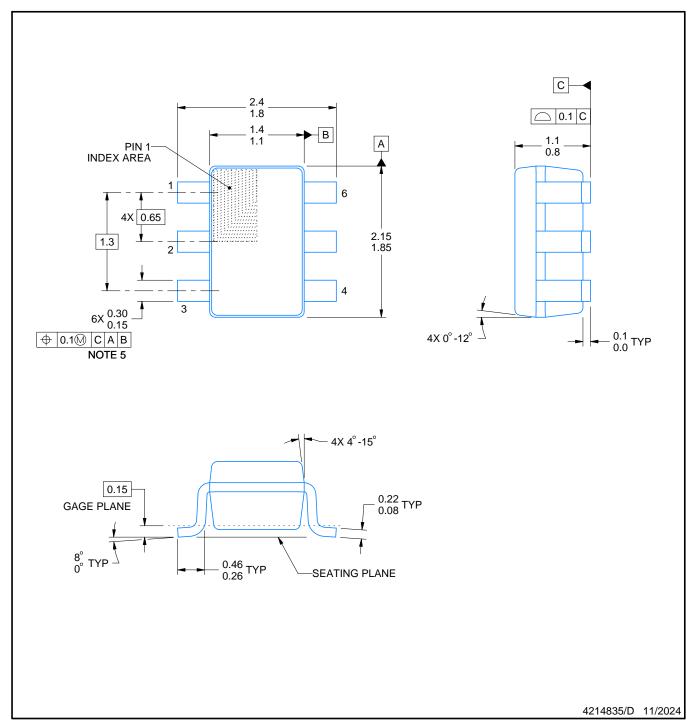
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





SMALL OUTLINE TRANSISTOR



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

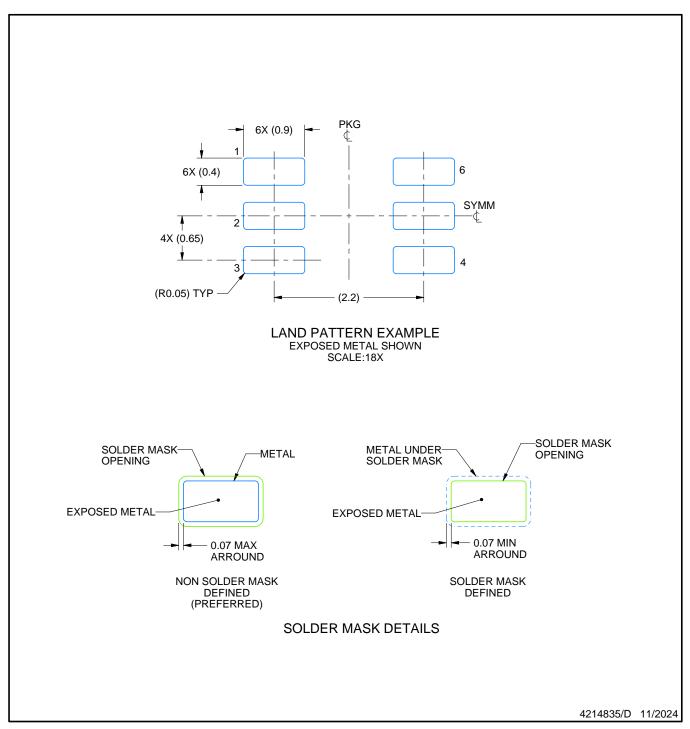
  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

  4. Falls within JEDEC MO-203 variation AB.



SMALL OUTLINE TRANSISTOR



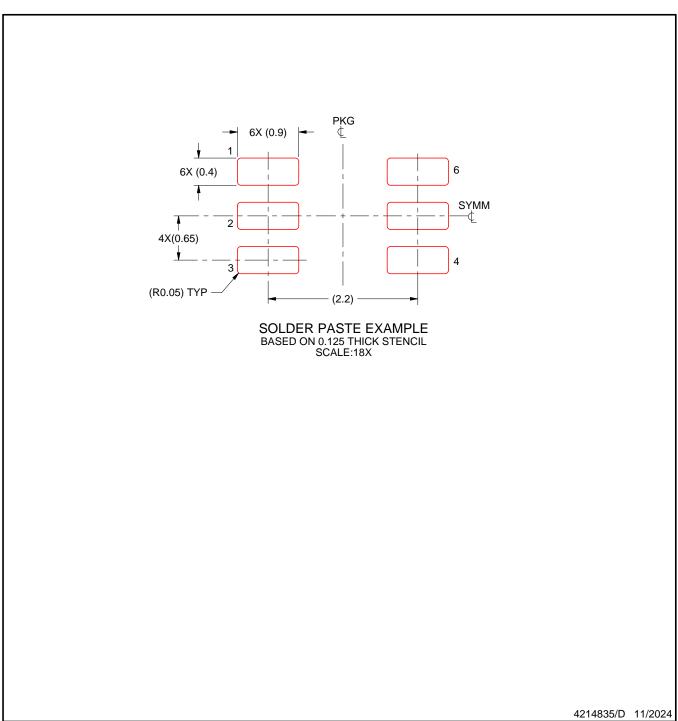
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



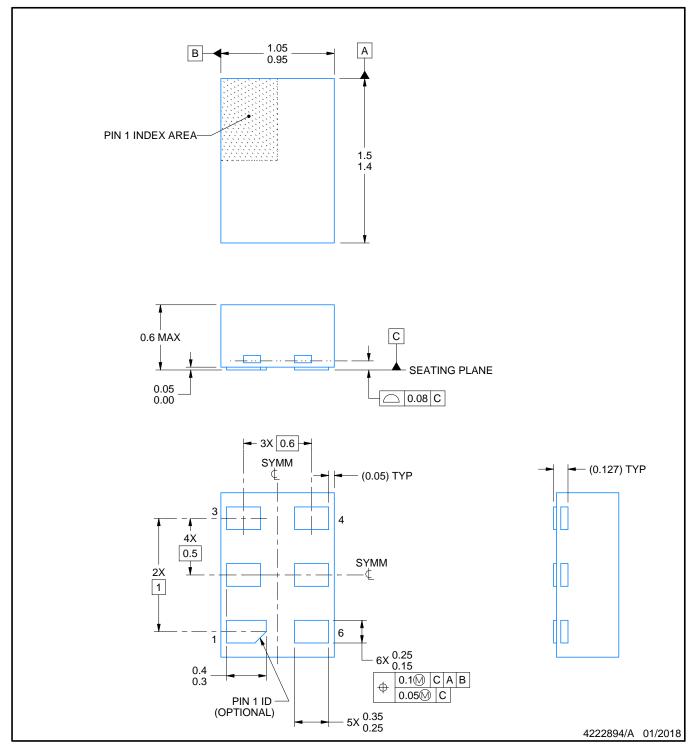


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4207181/G



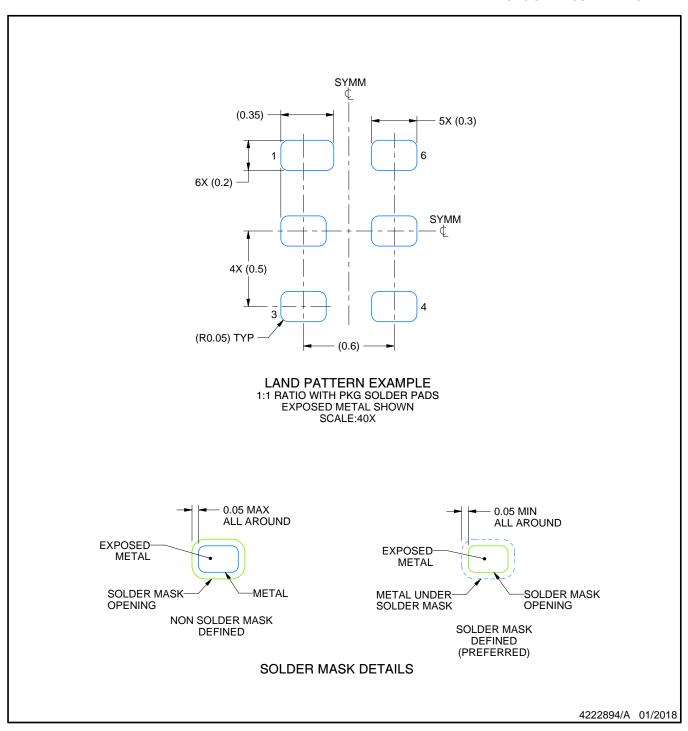




- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

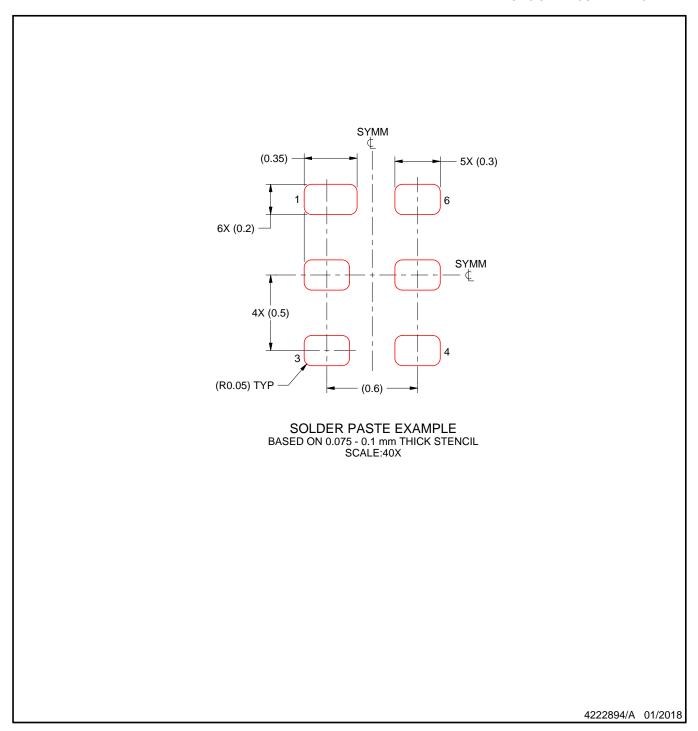




NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



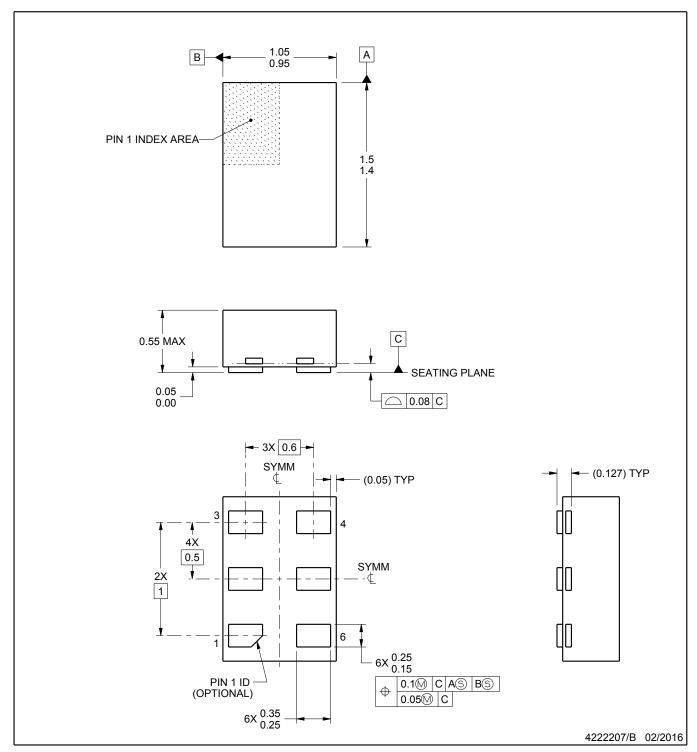


NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



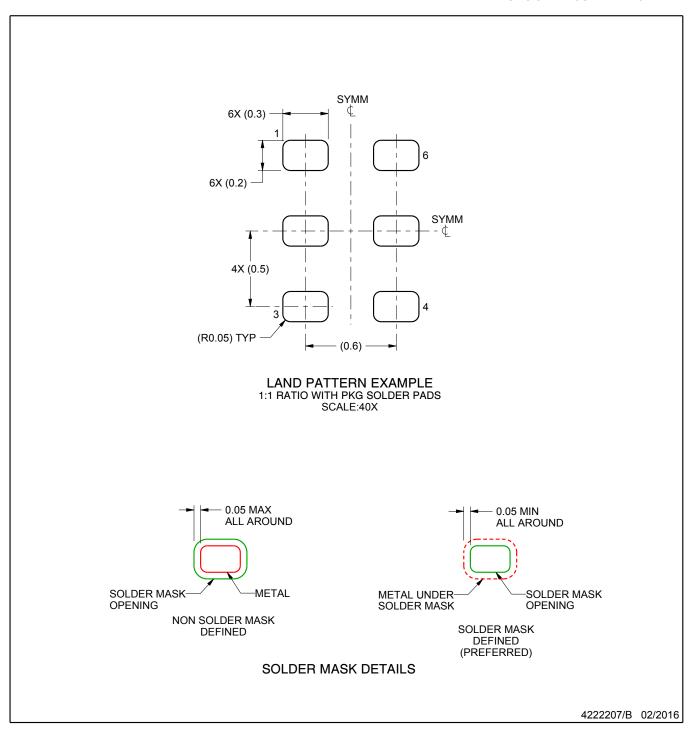




- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

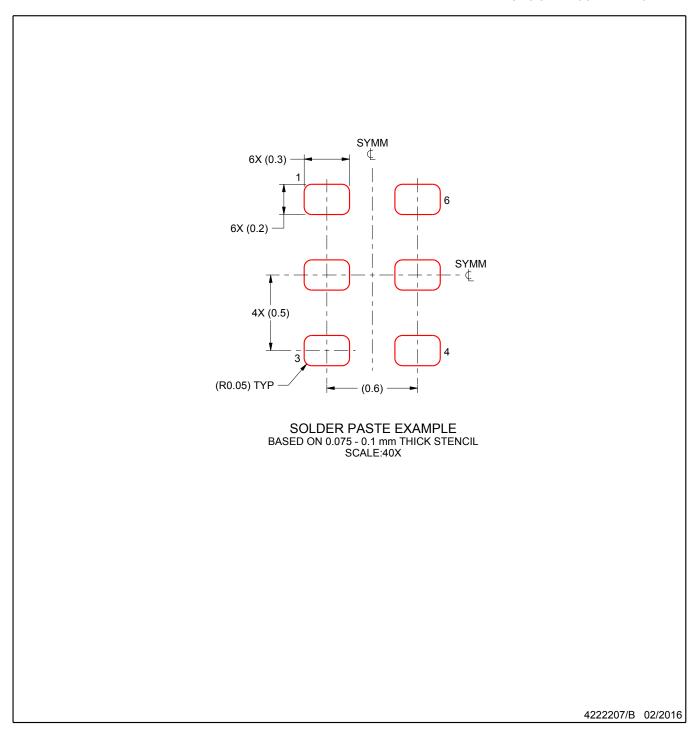




NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



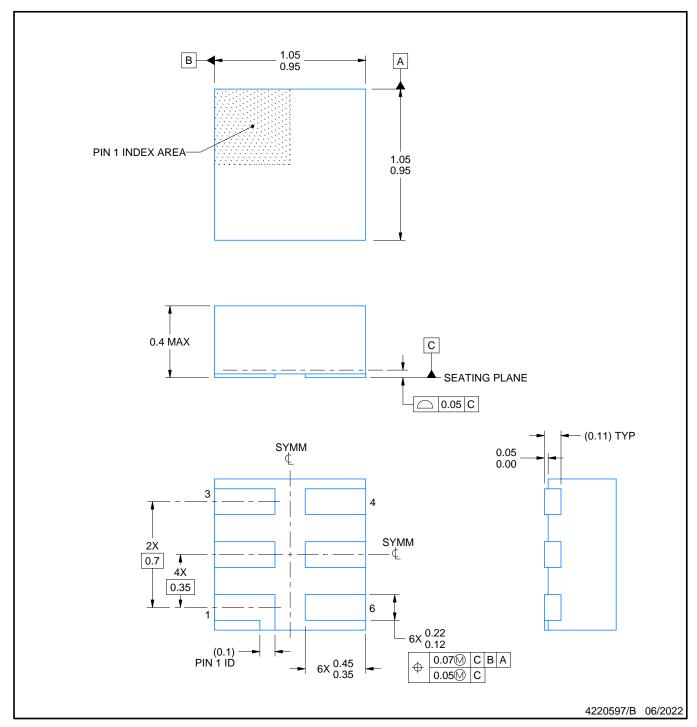


NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





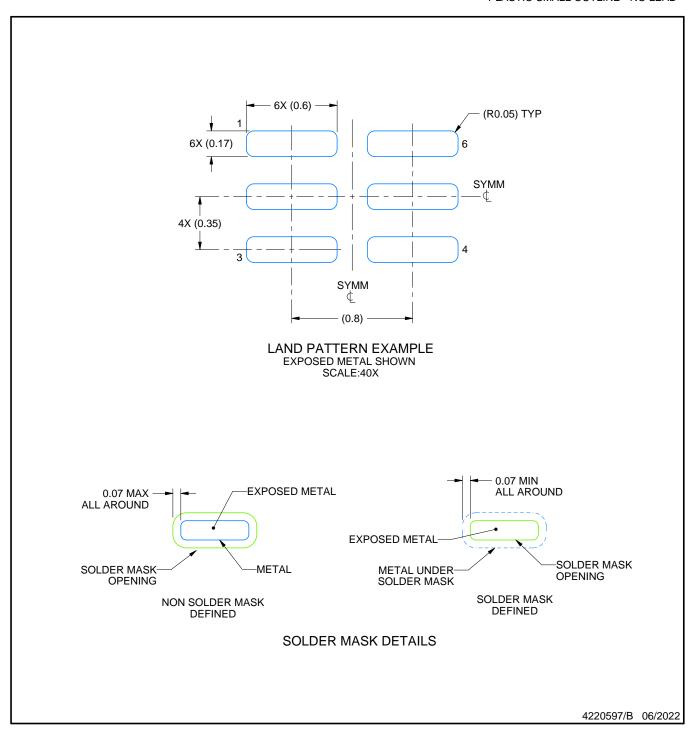


- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Reference JEDEC registration MO-287, variation X2AAF.

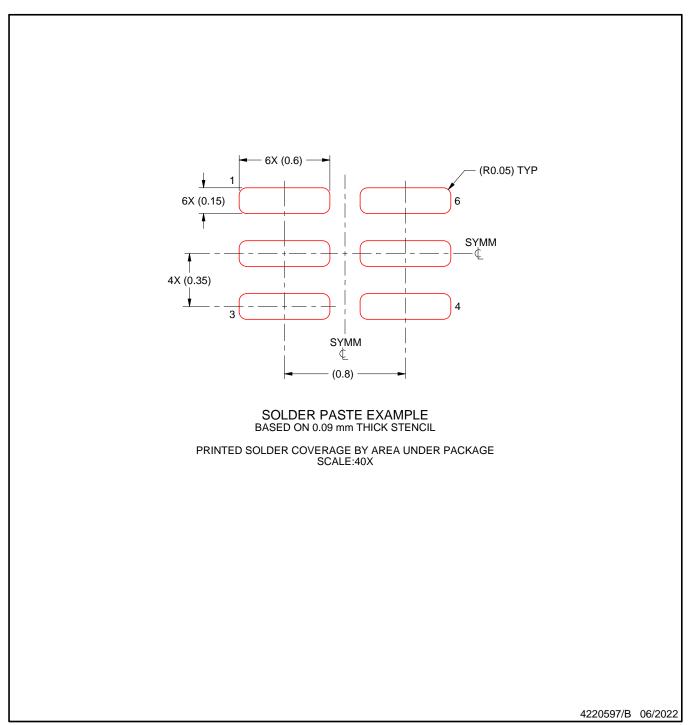




NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

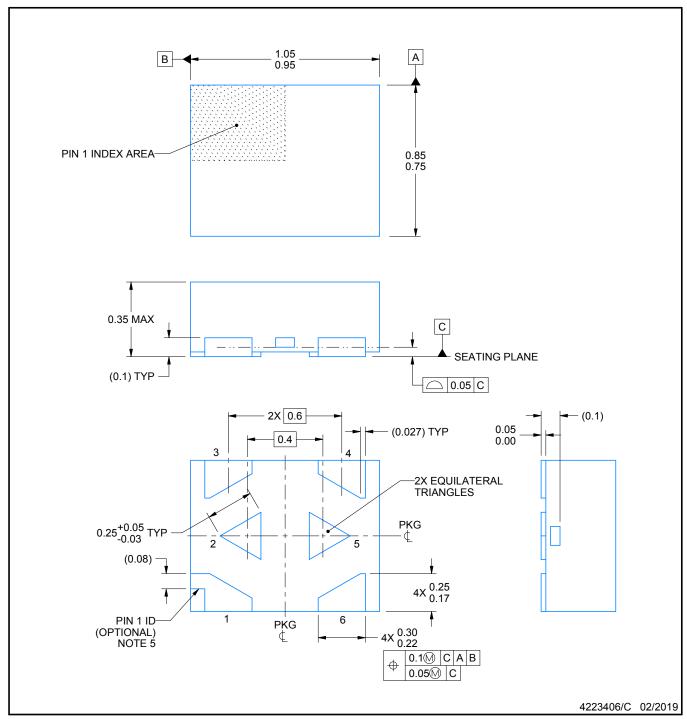




4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



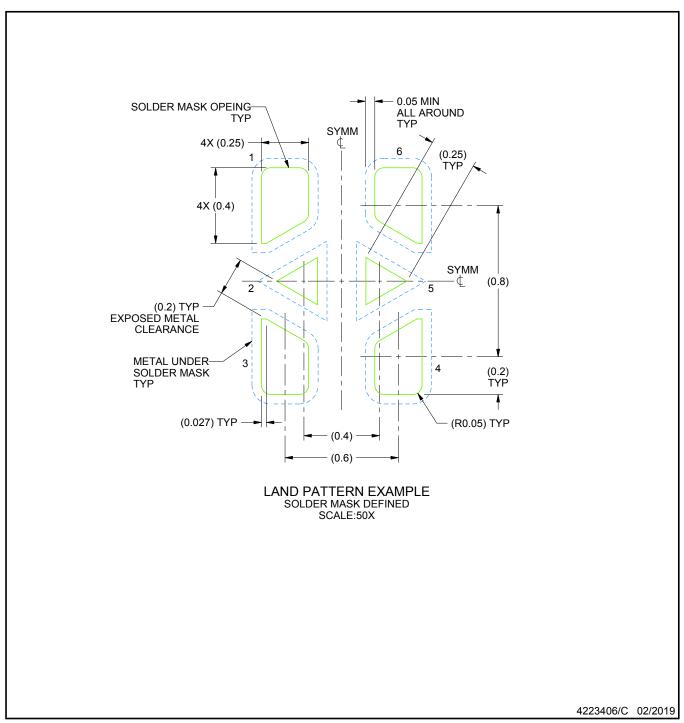




- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

  4. The size and shape of this feature may vary.
- 5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.



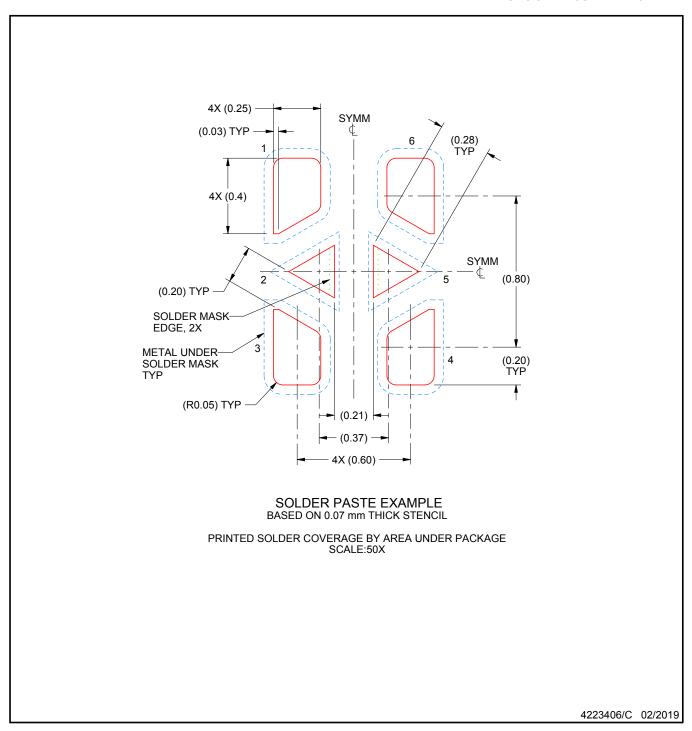


NOTES: (continued)



<sup>6.</sup> This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

<sup>7.</sup> Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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