

8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

features

- 8-Bit Resolution
- Differential Linearity Error
 - ±0.3 LSB Typ, ±1 LSB Max (25°C)
 ±1 LSB Max
- Integral Linearity Error
 - − ±0.6 LSB, ±0.75 LSB Max (25°C)
 − ±1 LSB Max
- Maximum Conversion Rate of 40 Megasamples Per Second (MSPS) Max
- Internal Sample and Hold Function
- 5-V Single Supply Operation
- Low Power Consumption . . . 85 mW Typ
- Analog Input Bandwidth . . . ≥75 MHz Typ
- Internal Reference Voltage Generators

applications

- Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK) Demodulators
- Digital Television
- Charge-Coupled Device (CCD) Scanners
- Video Conferencing
- Digital Set-Top Box
- Digital Down Converters
- High-Speed Digital Signal Processor Front End

description

The TLC5540 is a high-speed, 8-bit analog-to-digital converter (ADC) that converts at sampling rates up to 40 megasamples per second (MSPS). Using a semiflash architecture and CMOS process, the TLC5540 is able to convert at high speeds while still maintaining low power consumption and cost. The analog input bandwidth of 75 MHz (typ) makes this device an excellent choice for undersampling applications. Internal resistors are provided to generate 2-V full-scale reference voltages from a 5-V supply, thereby reducing external components. The digital outputs can be placed in a high impedance mode. The TLC5540 requires only a single 5-V supply for operation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

		nd di P VI		
OE [1	U	24] DGND
DGND [2		23] REFB
D1(LSB)	3		22] REFBS
D2 [4		21] AGND
D3 [5		20] AGND
D4 [6		19	ANALOG IN
D5 [7		18] V _{DDA}
D6 [8		17] REFT
D7 [9		16] REFTS
D8(MSB)	10		15	V _{DDA}
V _{DDD} [11		14] V _{DDA}
CLK [12		13	VDDD

DW OD NS DACKACE

AVAILABLE OPTIONS

_	PACKAGE					
TA	TSSOP (PW)	SOP (NS)				
−0°C to 70°C	TLC5540CPW	TLC5540CNSLE				
-40°C to 85°C	TLC5540IPW	TLC5540INSLE				

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functional block diagram



schematics of inputs and outputs



Terminal Functions

TERM	INAL		
NAME	NO.	1/0	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	Ι	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1-D8	3-10	0	Digital data out. D1:LSB, D8:MSB
OE	1	I	Output enable. When $\overline{OE} = L$, data is enabled. When $\overline{OE} = H$, D1–D8 is high impedance.
V _{DDA}	14, 15, 18		Analog V _{DD}
V _{DDD}	11, 13		Digital V _{DD}
REFB	23	I	ADC reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, the REFBS terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 13 and Figure 14).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, the REFTS terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 13 and Figure 14).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DDA} , V _{DDD}	
Reference voltage input range, VI(REFT), VI(REFB), VI(REFBS), VI(REFTS)	
Analog input voltage range, V _{I(ANLG)}	
Digital input voltage range, VI(DGTL)	DGND to V _{DDD}
Digital output voltage range, V _{O(DGTL)}	DGND to V _{DDD}
Operating free-air temperature range, T _A : TLC5540C	0°C to 70°C
TLC5540I	–40°C to 85°C
Storage temperature range, T _{stg}	–55°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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recommended operating conditions

			MIN	NOM	MAX	UNIT
	V _{DDA} -AGND		4.75	5	5.25	
Supply voltage	V _{DDD} -AGND	V _{DDD} -AGND		5	5.25	V
	AGND-DGND		-100	0	100	mV
Reference input voltage (top), VI(REFT)		V _{I(REFB)} +1.8	V _{I(REFB)} +2	V _{DDA}	V
Reference input voltage (bottom), VI(RI	EFB)		0	0.6	VI(REFT)-1.8	V
Analog input voltage range, VI(ANLG)	see Note 1)		VI(REFB)		VI(REFT)	V
Full scale voltage, VI(REFT) - VI(REFE	3)		1.8		5	V
High-level input voltage, VIH			4			V
Low-level input voltage, VIL					1	V
Pulse duration, clock high, $t_{W(H)}$			12.5			ns
Pulse duration, clock low, tw(L)			12.5			ns
	TLC5540C	TLC5540C			70	°C
Operating free-air temperature, T_A	TLC5540I	TLC5540I			85	°C

(1) $1.8 V \le V_{I(REFT)} - V_{I(REFB)} < V_{DD}$



electrical characteristics at $V_{DD} = 5 \text{ V}$, $V_{I(REFT)} = 2.6 \text{ V}$, $V_{I(REFB)} = 0.6 \text{ V}$, $f_s = 40 \text{ MSPS}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TES	MIN	TYP	MAX	UNIT	
-	I to contract the second second		$T_A = 25^{\circ}C$		±0.6	±1	
EL	Linearity error, integral	f _S = 40 MSPS,	$T_A = MIN$ to MAX			±1	
-		$V_{I} = 0.6 \text{ V to } 2.6 \text{ V}$	$T_A = 25^{\circ}C$		±0.3	±0.75	LSB
ED	Linearity error, differential		$T_A = MIN$ to MAX			±1	
	Self bias (1), V _{RB}	Short REFB to REFBS		0.57	0.61	0.65	
	Self bias (1), V _{RT}	Short REFT to REFTS	See Figure 13	2.47	2.63	2.80	.,
	Self bias (2), V _{RB}	Short REFB to AGND			AGND		V
	Self bias (2), V _{RT}	Short REFT to REFTS	See Figure 14	2.18	2.29	2.4	
I _{ref}	Reference-voltage current	VI(REFT) - VI(REFB) =	5.2	7.5	12	mA	
R _{ref}	Reference-voltage resistor	Between REFT and REF	165	270	350	Ω	
Ci	Analog input capacitance	V _{I(ANLG)} = 1.5 V + 0.07		4		pF	
E _{ZS}	Zero-scale error		-18	-43	-68		
E _{FS}	Full-scale error	$V_{I(REFT)} - V_{I(REFB)} =$	2 V	-25	0	25	mV
Iн	High-level input current	V _{DD} = 5.25 V,	$V_{IH} = V_{DD}$			5	
۱ _{IL}	Low-level input current	V _{DD} = 5.25 V,	$V_{IL} = 0$			5	μA
IOH	High-level output current	OE = GND,	$V_{DD} = 4.75 \text{ V}, V_{OH} = V_{DD} - 0.5 \text{ V}$	-1.5			
IOL	Low-level output current	OE = GND,	$V_{DD} = 4.75 \text{ V}, V_{OL} = 0.4 \text{ V}$	2.5			mA
IOZH(lkg)	High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V _{DD} = 5.25, V _{OH} = V _{DD}			16	
IOZL(lkg)	Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD},$	V _{DD} = 4.75, V _{OL} = 0			16	μA
IDD	Supply current	$f_{S} = 40 \text{ MSPS}, C_{L} \le 25 \text{ p}$ NTSC [‡] ramp wave inpu			17	27	mA

[†]Conditions marked MIN or MAX are as stated in recommended * National Television System Committee
 Supply current specification does not include I_{ref}.



operating characteristics at V_{DD} = 5 V, V_{RT} = 2.6 V, V_{RB} = 0.6 V, f_s = 40 MSPS, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST C	CONDITIONS [†]	MIN	TYP	MAX	UNIT	
f _s	Maximum conversion rate	$T_A = MIN \text{ to } MA$	$T_A = MIN$ to MAX				MSPS	
f _S	Minimum conversion rate	$T_A = MIN \text{ to } MA$	$T_A = MIN \text{ to MAX}$		5		MSPS	
BW	Analog input full-power bandwidth	At – 3 dB,	VI(ANLG) = 2 V _{pp}		75		MHz	
tpd	Delay time, digital output	$C_L \le 10 \text{ pF}$ (see			9	15	ns	
t _{PHZ}	Disable time, output high to Hi-Z	C _L ≤ 15 pF,	$I_{OH} = -4.5 \text{ mA}$			20	ns	
t _{PLZ}	Disable time, output low to Hi-Z	C _L ≤ 15 pF,	I _{OL} = 5 mA			20	ns	
^t PZH	Enable time, Hi-Z to output high	C _L ≤ 15 pF,	$I_{OH} = -4.5 \text{ mA}$			15	ns	
tPZL	Enable time, Hi-Z to output low	C _L ≤ 15 pF,	IOL = 5 mA			15	ns	
	Differential gain	NTSC 40 IRE [‡]	modulation wave,		1%			
	Differential phase	f _S = 14.3 MSPS			0.7		degrees	
t _{AJ}	Aperture jitter time				30		ps	
^t d(s)	Sampling delay time				4		ns	
			f _l = 1 MHz		47			
			fl = 3 MHz	44	47			
		f _S = 20 MSPS	fl = 6 MHz		46			
SNR	Signal-to-noise ratio		f _l = 10 MHz		45		dB	
			fl = 3 MHz		45.2		7	
		f _S = 40 MSPS	fl = 6 MHz	42	44			
			f _l = 10 MHz		42			
			fl = 1 MHz		7.64			
		(fl = 3 MHz		7.61		1	
	F7 (1)	f _S = 20 MSPS	f _l = 6 MHz		7.47			
ENOB	Effective number of bits		f _l = 10 MHz		7.16	Bits		
		(fl = 3 MHz		7		1	
		f _S = 40 MSPS	fl = 6 MHz		6.8]	
			f _l = 1 MHz		43			
		6 00 MODO	fl = 3 MHz	35	42			
	Total homeonic distortion	f _S = 20 MSPS	fl = 6 MHz		41		dBc	
THD	Total harmonic distortion		fl = 10 MHz		38			
		f _ 40 MODO	fl = 3 MHz		40			
		f _S = 40 MSPS	fl = 6 MHz		38			
	Spurious-free dynamic range	$f_S = 20 MSPS$	fi – 3 MHz	41	46		dBc	
	Spurious-free dynamic range	f _S = 40 MSPS	f _l = 3 MHz		42		UDC	

[†] Conditions marked MIN or MAX are as stated in recommended operating conditions.
 [‡] Institute of Radio Engineers
 (2) C_L includes probe and jig capacitance.



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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS





APPLICATION INFORMATION

grounding and power supply considerations

A signal ground is a low-impedance path for current to return to the source. Inside the TLC5540 A/D converter, the analog ground and digital ground are connected to each other through the substrate, which has a very small resistance (~30 Ω) to prevent internal latch-up. For this reason, it is strongly recommended that a printed circuit board (PCB) of at least 4 layers be used with the TLC5540 and the converter DGND and AGND pins be connected directly to the analog ground plane to avoid a ground loop. Figure 11 shows the recommended decoupling and grounding scheme for laying out a multilayer PC board with the TLC5540. This scheme ensures that the impedance connection between AGND and DGND is minimized so that their potential difference is negligible and noise source caused by digital switching current is eliminated.



Figure 11. AV_{DD}, DV_{DD}, AGND, and DGND Connections

printed circuit board (PCB) layout considerations

When designing a circuit that includes high-speed digital and precision analog signals such as a high speed ADC, PCB layout is a key component to achieving the desired performance. The following recommendations should be considered during the prototyping and PCB design phase:

- Separate analog and digital circuitry physically to help eliminate capacitive coupling and crosstalk. When separate analog and digital ground planes are used, the digital ground and power planes should be several layers from the analog signals and power plane to avoid capacitive coupling.
- Full ground planes should be used. Do not use individual etches to return analog and digital currents or partial ground planes. For prototyping, breadboards should be constructed with copper clad boards to maximize ground plane.
- The conversion clock, CLK, should be terminated properly to reduce overshoot and ringing. Any jitter on the conversion clock degrades ADC performance. A high-speed CMOS buffer such as a 74ACT04 or 74AC04 positioned close to the CLK terminal can improve performance.
- Minimize all etch runs as much as possible by placing components very close together. It also proves beneficial to place the ADC in a corner of the PCB nearest to the I/O connector analog terminals.
- It is recommended to place the digital output data latch (if used) as close to the TLC5540 as possible to minimize capacitive loading. If D0 through D7 must drive large capacitive loads, internal ADC noise may be experienced.

PRINCIPLES OF OPERATION

functional description

The TLC5540 uses a modified semiflash architecture as shown in the functional block diagram. The four most significant bits (MSBs) of every output conversion result are produced by the upper comparator block CB1. The four least significant bits (LSBs) of each alternate output conversion result are produced by the lower comparator blocks CB-A and CB-B in turn (see Figure 12).

The reference voltage that is applied to the lower comparator resistor string is one sixteenth of the amplitude of the reference applied to the upper comparator resistor string. The sampling comparators of the lower comparator block require more time to sample the lower voltages of the reference and residual input voltage. By applying the residual input voltage to alternate lower comparator blocks, each comparator block has twice as much time to sample and convert as would be the case if only one lower comparator block were used.



Figure 12. Internal Functional Timing Diagram

This conversion scheme, which reduces the required sampling comparators by 30 percent compared to standard semiflash architectures, achieves significantly higher sample rates than the conventional semiflash conversion method.



PRINCIPLES OF OPERATION

functional description (continued)

The MSB comparator block converts on the falling edge of each applied clock cycle. The LSB comparator blocks CB-A and CB-B convert on the falling edges of the first and second following clock cycles, respectively. The timing diagram of the conversion algorithm is shown in Figure 12.

analog input operation

The analog input stage to the TLC5540 is a chopper-stabilized comparator and is equivalently shown below:



Figure 13. External Connections for Using the Internal Reference Resistor Divider

Figure 13 depicts the analog input for the TLC5540. The switches shown are controlled by two internal clocks, $\phi 1$ and $\phi 2$. These are nonoverlapping clocks that are generated from the CLK input. During the sampling period, $\phi 1$, S1 is closed and the input signal is applied to one side of the sampling capacitor, C_S. Also during the sampling period, S2 through S(N) are closed. This sets the comparator input to approximately 2.5 V. The delta voltage is developed across C_S. During the comparison phase, $\phi 2$, S1 is switched to the appropriate reference voltage for the bit value N. S2 is opened and V_{ref(N)} – VC_S toggles the comparator output to the appropriate digital 1 or 0. The small resistance values for the switch, S1, and small value of the sampling capacitor combine to produce the wide analog input bandwidth of the TLC5540. The source impedance driving the analog input of the TLC5540 should be less than 100 Ω across the range of input frequency spectrum.

reference inputs - REFB, REFT, REFBS, REFTS

The range of analog inputs that can be converted are determined by REFB and REFT, REFT being the maximum reference voltage and REFB being the minimum reference voltage. The TLC5540 is tested with REFT = 2.6 V and REFB = 0.6 V producing a 2-V full-scale range. The TLC5540 can operate with REFT – REFB = 5 V, but the power dissipation in the reference resistor increases significantly (93 mW nominally). It is recommended that a 0.1 μ F capacitor be attached to REFB and REFT whether using externally or internally generated voltages.

PRINCIPLES OF OPERATION

internal reference voltage conversion

Three internal resistors allow the device to generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND. Two different bias voltages are possible without the use of external resistors.

Internal resistors are provided to develop REFT = 2.6 V and REFB = 0.6 V (bias option one) with only two external connections. This is developed with a 3-resistor network connected to V_{DDA}. When using this feature, connect REFT to REFTS and connect REFB to REFBS. For applications where the variance associated with V_{DDA} is acceptable, this internal voltage reference saves space and cost (see Figure 14).

A second internal bias option (bias two option) is shown in Figure 15. Using this scheme REFB = AGND and REFT = 2.28 V nominal. These bias voltage options can be used to provide the values listed in the following table.

BIAS OPTION	BIAS VOLTAGE						
BIAS OPTION	V _{RB}	V _{RT}	V _{RT} – V _{RB}				
1	0.61	2.63	2.02				
2	AGND	2.28	2.28				

Table 1. Bias Voltage Options

To use the internally-generated reference voltage, terminal connections should be made as shown in Figure 14 or Figure 15. The connections in Figure 14 provide the standard video 2-V reference.



Figure 14. External Connections Using the Internal Bias One Option



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PRINCIPLES OF OPERATION





functional operation

Table 2 shows the TLC5540 functions.

INPUT SIGNAL				DIG	ITAL OU	TPUT C	ODE		
VOLTAGE	STEP	MSB							LSB
V _{ref(T)}	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
V _{ref(B)}	0	0	0	0	0	0	0	0	0

Table 2. Functional Operation



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TLC5540CNS.A	Active	Production	SOP (NS) 24	34 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5540
TLC5540CPW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	P5540
TLC5540CPW.A	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	P5540
TLC5540INS.A	Active	Production	SOP (NS) 24	34 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5540I
TLC5540INSR	Active	Production	SOP (NS) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5540I
TLC5540INSR.A	Active	Production	SOP (NS) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5540I
TLC5540IPW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540
TLC5540IPW.A	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540
TLC5540IPWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540
TLC5540IPWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE OPTION ADDENDUM

30-Jun-2025

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All di	imensions are nominal												
	Device	•	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TLC5540INSR	SOP	NS	24	2000	330.0	24.4	8.5	15.3	2.6	12.0	24.0	Q1
	TLC5540IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



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PACKAGE MATERIALS INFORMATION

23-May-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5540INSR	SOP	NS	24	2000	350.0	350.0	43.0
TLC5540IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TEXAS INSTRUMENTS

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TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
TLC5540CNS.A	NS	SOP	24	34	530	10.5	4000	4.1
TLC5540CPW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5540CPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5540INS.A	NS	SOP	24	34	530	10.5	4000	4.1
TLC5540IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5540IPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0014A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0014A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
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- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0024A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

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7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0024A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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