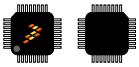
KV5x Data Sheet

240 MHz Cortex-M7 based MCU for Real-time, high performance connected control

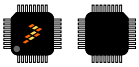
The Kinetis KV5x family of MCU is a high-performance solution offering exceptional precision, sensing, and control targeting Motor Control, Industrial Drives and Automation, and Power Conversion. Apart from the high performance Cortex-M7 core, it features top notch real time control peripherals such as high resolution pulse-width modulation (PWM) with 260 ps resolution, 4 Fast 12-bit ADCs with 5 MSps, up to 44 PWM channels for supporting multi-motor systems. It also comes with multiple communication peripherals including 3 FlexCAN modules, optional Ethernet Communications, and multiple UART, SPI, and I2C modules. The KV5x is supported by a comprehensive enablement suite from NXP and third-party resources including reference designs, software libraries, and motor configuration tools.

MKV58F1M0Vxx24
MKV56F1M0Vxx24
MKV58F512Vxx24
MKV56F512Vxx24



144 LQFP
20 x 20 x 1.4 mm Pitch 0.5 mm

144 BGA
13 x 13 x 1.23 mm Pitch 1.0 mm



100 LQFP
14 x 14 x 1.4 mm Pitch 0.5 mm

Core

- ARM® Cortex®-M7 core up to 240 MHz with single precision Floating Point Unit (FPU)

Memories

- Up to 1 MB program flash memory
- Up to 256 KB RAM
- External memory interface (FlexBus)

System peripherals

- 32-channel DMA controller
- Low-leakage wakeup unit
- SWD debug interface
- Advanced independent clocked watchdog
- JTAG debug interface

Clocks

- 32 to 40 kHz or 3 to 32 MHz crystal oscillator
- MCG with FLL and PLL referencing internal or external reference clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Human-machine interface

- General-purpose input/output

Communication interfaces

- Six UART/FlexSCI modules with programmable 8- or 9-bit data format
- Three 16-bit SPI modules
- Two I2C modules
- Three FlexCAN modules
- Ethernet Module (Optional)

Analog Modules

- Four 12-bit SAR High Speed ADCs with 5 MSPS sample rate
- One 16-bit ADC
- Four CMPs with a 6-bit DAC and programmable reference input
- One 12-bit DAC

Timers

- Two eflexPWM with 4 sub-modules, with 12 PWM outputs, one eflexPWM module with less than 285 ps resolution provided by nano-edge module.
- Two 8-channel FlexTimers (FTM0 and FTM3)
- Two 2-channel FlexTimers (FTM1 and FTM2)
- Four Periodic interrupt timers (PIT)
- Two Programmable Delay Blocks (PDB)
- Quadrature Encoder/Decoder (ENC)

Security and integrity modules

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Hardware CRC module to support fast cyclic redundancy checks
- External Watchdog Monitor (EWM)
- True Random Number Generator (TRNG)
- Memory mapped Cryptographic Acceleration Unit (MMCAU)
- Advanced Watchdog (WDOG) timer modules

Orderable part numbers summary[1]

NXP part number	CPU frequency (MHz)	Ambient operating temperature (°C)	Package	Flash/ SRAM	Ethernet	CAN	GPIO
MKV58F1M0VMD24[2]	240	105	144 MAPBGA	1 MB/256 KB	Yes	3	111
MKV58F1M0VLQ24	240	105	144 LQFP	1 MB/256 KB	Yes	3	111
MKV58F1M0VLL24	240	105	100 LQFP	1 MB/256 KB	Yes	3	74
MKV56F1M0VMD24[2]	240	105	144 MAPBGA	1 MB/256 KB	No	2	111
MKV56F1M0VLQ24	240	105	144 LQFP	1 MB/256 KB	No	2	111
MKV56F1M0VLL24	240	105	100 LQFP	1 MB/256 KB	No	2	74
MKV58F512VMD24[2]	240	105	144 MAPBGA	512 KB/128 KB	Yes	3	111
MKV58F512VLQ24	240	105	144 LQFP	512 KB/128 KB	Yes	3	111
MKV58F512VLL24	240	105	100 LQFP	512 KB/128 KB	Yes	3	74
MKV56F512VMD24[2]	240	105	144 MAPBGA	512 KB/128 KB	No	2	111
MKV56F512VLQ24	240	105	144 LQFP	512 KB/128 KB	No	2	111
MKV56F512VLL24	240	105	100 LQFP	512 KB/128 KB	No	2	74

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.
2. The 144-pin MAPBGA package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor

Table continues on the next page...

Related Resources (continued)

Type	Description	Resource
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV5XP144M240RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KV5XP144M240[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_V_0N86P[1] KINETIS_V_1N86P[1]
Package drawing	Package dimensions are provided in package drawings.	• MAPBGA 144-pin: 98ASA00222D[1] • LQFP 144-pin: 98ASS23177W[1] • LQFP 100-pin: 98ASS23308W[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

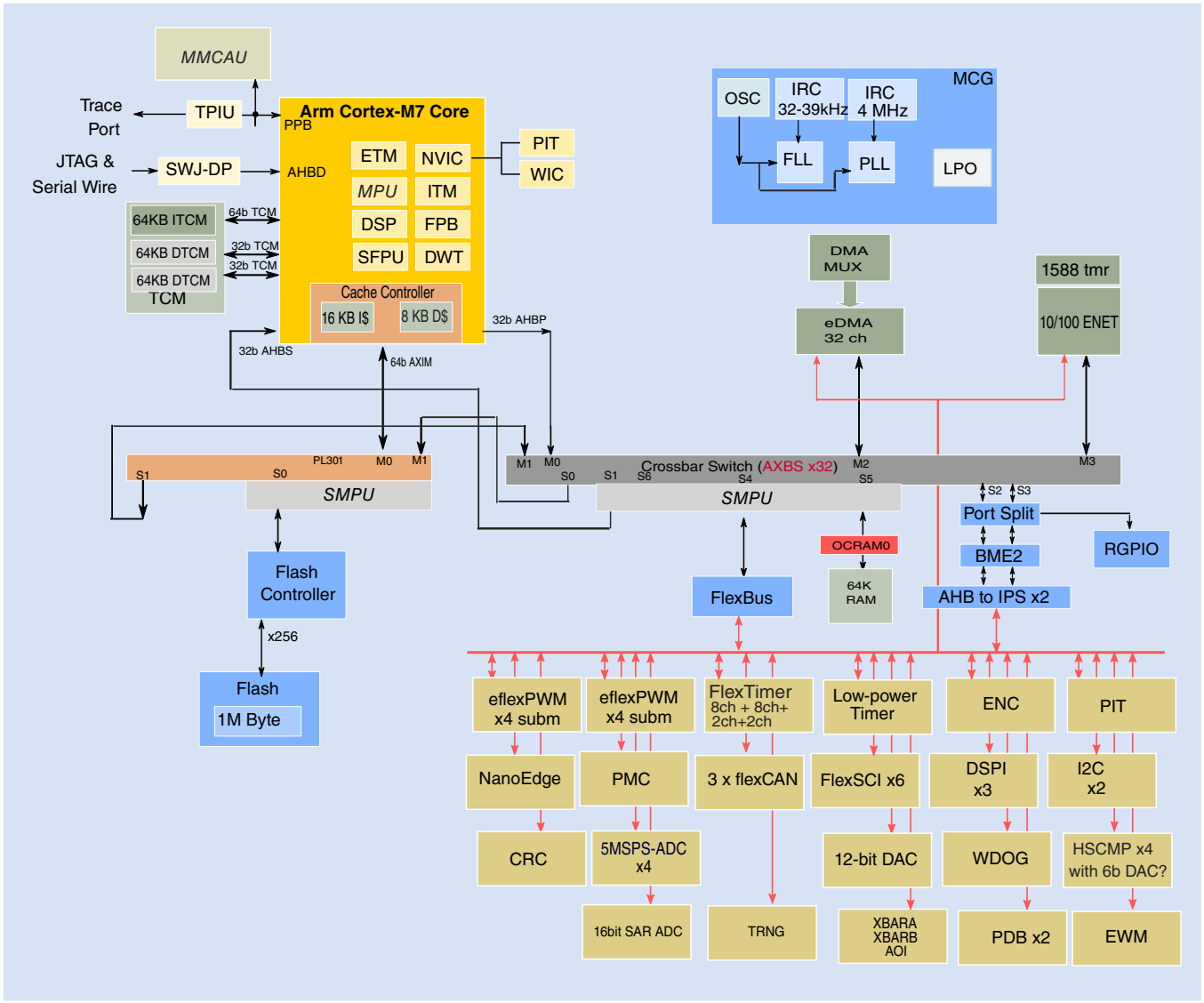


Figure 1. KV5x block diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	220[1]	mA
V_{IO}	Pin input voltage	–0.3	3.8[2]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage[3]	V_{DD} – 0.3	V_{DD} + 0.3	V

1. All V_{DD}/V_{SS} pins must be utilized for this value to be valid.
2. Maximum value of V_{IO} must be 3.8 V.
3. Limits on V_{DDA} also apply to V_{REFH}.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

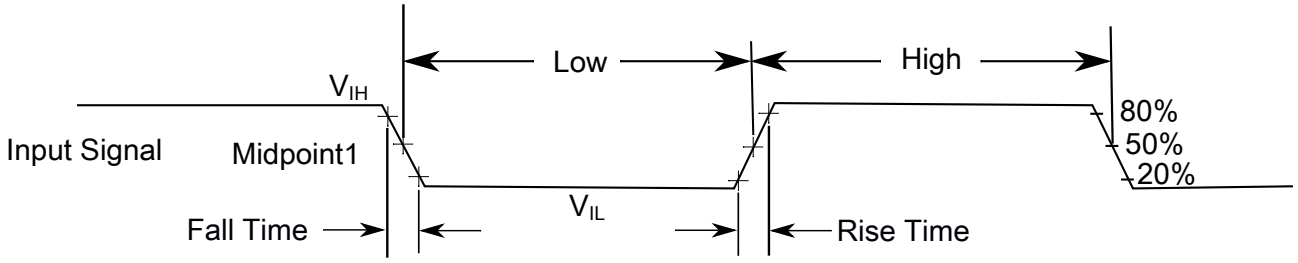


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 1. Voltage and current operating requirements (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Symbol	Description	Notes[1]	Min	Max	Unit	
V_{DD}	Digital supply voltage		1.71	3.6	V	
V_{DDA}	Analog supply voltage		V_{DD}	3.6	V	
V_{REFHx}	ADC Reference Voltage High		1.8	V_{DDA}	V	
ΔVDD	Voltage difference V_{DD} to V_{DDA}		-0.1	0.1	V	
ΔVSS	Voltage difference V_{SS} to V_{SSA}		-0.1	0.1	V	
V_{IH}	Input Voltage High (digital inputs) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V		 0.7 x V_{DD} 0.75 x V_{DD}	 — —	V V	
V_{IL}	Input Voltage Low (digital inputs) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V		 — —	 0.35 x V_{DD} 0.3 x V_{DD}	V	
I_{ICIO}	IO pin negative DC injection current – single pin. V_{IN} < V_{SS} – 0.3V	-3	—	—	mA	2
I_{ICcont}	Contiguous pin DC injection current – regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
   - Pin Group 6: PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. have high output current capability
2. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is greater than V_{IO_MIN} (= V_{SS}-0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.

2.2.2 HVD, LVD, and POR operating requirements

Table 2. V_{DD} supply HVD, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

Table 2. V_{DD} supply HVD, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{HVDH}	High Voltage Detect (High Trip Point)	—	3.7202	—	V	
V_{HVDL}	High Voltage Detect (Low Trip Point)	—	3.4582	—	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	—	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	—	V	
V_{OH}	Output high voltage — High drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	—	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	—	V	

Table continues on the next page...

Table 3. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	—	0.5	V	
V_{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	—	0.5	V	
V_{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 3 mA	—	—	0.5	V	
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	µA	1, 2
	High drive port pins	—	0.004	0.5	µA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	—	V_{DD}	mA	3
R_{PU}	Internal pullup resistors	20	—	50	kΩ	4
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	5

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at VDD=3.6V
3. Open drain outputs must be pulled to V_{DD}.
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
5. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the	—	—	300	µs	

Table continues on the next page...

Table 4. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	first instruction across the operating temperature range of the chip.					
	• VLLS0 → RUN	—	—	149	µs	
	• VLLS1 → RUN	—	—	149	µs	
	• VLLS3 → RUN	—	—	79	µs	
	• VLPS → RUN	—	—	5.7	µs	
	• STOP → RUN	—	—	5.7	µs	

2.2.5 Power consumption operating behaviors

NOTE

In the following table, the maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3σ).

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	5	8	mA	HSADC0 and HSADC1 with 66.6 MHz clock, ADC0 with 25 MHz clock.
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, while(1) loop, excludes ADC IDDA					Core frequency of 25 MHz
	• @ 1.8V	—	7.5	36	mA	
	• @ 3.0V	—	7.6	39	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, while(1) loop, excludes ADC IDDA					Core frequency of 50 MHz
	• @ 1.8V	—	10.8	—	mA	
	• @ 3.0V	—	10.8	—	mA	

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, while(1) loop, excludes ADC IDDA • @ 3.0V • @25°C • @105°C	 — —	 27.9 44.3	 30.0 55.7	 mA mA	Core frequency of 160 MHz.
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, running benchmark code from flash, excludes ADC IDDA • @ 3.0V • @25°C • @105°C	 — —	 70.0 79.9	 — —	 mA mA	CoreMark benchmark compiled using IAR 7.50 with optimization level set to High for Speed with no size constraints option selected. Clock frequencies configured as follows: • Core clock is 160 MHz • Fast Peripheral clock is 80 MHz • Flexbus clock is 26.67 MHz • Bus/ Flash clock is 26.67 MHz
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash, while(1) loop, excludes ADC IDDA • @ 3.0V • @25°C • @105°C	 — —	 43.8 62.5	 47.1 80.8	 mA mA	Core frequency of 240 MHz.
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash, while(1) loop, excludes ADC IDDA • @ 3.0V					Core frequency of 240 MHz. Nanoedge module at 120 MHz.

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 25°C	—	70.8	74.1	mA	
	• @ 105°C	—	92.3	107.9	mA	
I_{DD_HSRUN}	HSRun mode current — all peripheral clocks disabled, running benchmark code from flash, excludes ADC IDDA • @ 3.0V • @ 25°C • @ 105°C	— —	116 132.9	— —	mA mA	CoreMark benchmark compiled using IAR 7.50 with optimization level set to High for Speed with no size constraints option selected. Clock frequencies configured as follows: • Core clock is 240 MHz • Fast Peripheral clock is 120 MHz • Flexbus clock is 30 MHz • Bus/ Flash clock is 24 MHz
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	16.3	—	mA	160 MHz PEE mode, Fast Peripheral clock = 80 MHz, Flexbus clock = 80 MHz, Bus/ Flash clock = 20 MHz
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.729	7.6	mA	CPU frequency 4 MHz
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.2	9.4	mA	CPU frequency 4 MHz
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.33	0.43	mA	4 MHz System/ Core clock, Fast peripheral clock, and Flexbus clock.

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
						1 MHz bus/ flash clock. All peripheral clocks disabled. Temp = 25°C.
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.55	0.91	mA	
	• @ 105°C	—	11.1	18.3	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.107	0.33	mA	
	• @ 105°C	—	4.0	7.6	mA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	5.2	8.6	µA	
	• @ 70°C	—	29.8	85	µA	
	• @ 105°C	—	122.4	185	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	3.2	4.8	µA	
	• @ 70°C	—	11.6	45	µA	
	• @ 105°C	—	47.2	71	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	0.778	2.6	µA	
	• @ 70°C	—	3.9	21	µA	
	• @ 105°C	—	18.8	36	µA	
I_{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	0.5	2.1	µA	
	• @ 70°C	—	3.4	21	µA	
	• @ 105°C	—	18.2	36	µA	
I_{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.147	1.69	µA	
	• @ 70°C	—	3.0	16.8	µA	
	• @ 105°C	—	17.6	29.2	µA	

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	LLS	440	490	540	560	570	580	
	VLPS	490	490	540	560	570	680	
	STOP	510	560	560	560	610	680	
		510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Conditions	Clocks	Frequency band (MHz)	Typ.	Unit	Notes
V_{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. • Supply voltage VDD = 3.3 V • Temperature = 25 °C	• f_{OSC}= 20 MHz (crystal) • f_{SYS} = 150 MHz	0.15–50	14	dBµV	1
			50–150	25	dBµV	
			150–500	23	dBµV	
			500–1000	16	dBµV	
			0.15–1000	K	—	2

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{sys}	System (CPU) clock	—	240	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{sys}	System (CPU) clock	—	160	MHz	
$f_{FastPeripheral}$	Fast Peripheral Clock	—	120	MHz	1
FB_CLK	FlexBus clock	—	60	MHz	
f_{Bus_Flash}	Bus / Flash clock	—	27.5	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
VLPR mode					
f_{sys}	System (CPU) clock	—	4	MHz	
$f_{FastPeripheral}$	Fast Peripheral Clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{Bus_Flash}	Bus / Flash Clock	—	500	kHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	2

1. When using this clock to supply the nano-edge module, this clock must be 1/2 of the system clock.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is a clock input connected to the EXTAL pin with the OSC configured for bypass (external clock) operation.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, FlexCAN, and I^2C signals.

Table 10. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter enabled, analog filter disabled) — Asynchronous path	80	—	ns	2
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	2
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	10	—	ns	2
Port rise and fall times Normal drive fast pins				3, 4

Table continues on the next page...

Table 10. General switching specifications (continued)

Description	Min.	Max.	Unit	Notes

• 2.7≤ VDD ≤ 3.6 V
  • Fast slew rate
  • Slow slew rate
• 1.71≤ VDD < 2.7 V
  • Fast slew rate
  • Slow slew rate
	—
	—
	
		0.7
		16
		
		2.15
		16
			ns
			ns	

Port rise and fall times
High drive fast pins (normal/low drive enabled)
• 2.7≤ VDD ≤ 3.6 V
  • Fast slew rate
  • Slow slew rate
• 1.71≤ VDD < 2.7 V
  • Fast slew rate
  • Slow slew rate
	
	—
	—
	
		0.7
		15.65
		
		2.35
		35.3
			
			ns
			ns
			
				3, 5

Port rise and fall times
High drive fast pins (high drive enabled)
• 2.7≤ VDD ≤ 3.6 V
  • Fast slew rate
  • Slow slew rate
• 1.71≤ VDD < 2.7 V
  • Fast slew rate
  • Slow slew rate
	
	—
	—
	
		3
		16.5
		
		6.5
		36.3
			
			ns
			ns	

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (normal/low drive) is 25pF. Fast slew rate is enabled by clearing PORTx_PCRn[SRE].
4. Normal drive fast pins: All other GPIO pins that are not high drive fast pins.
5. High drive fast pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. High drive capability is enabled by setting PORTx_PCRn[DSE]

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	144 MAPBGA[1]	144 LQFP	100 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	—	51	51	°C/W	2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	—	42	38	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	42	41	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	36	32	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	—	30	23	°C/W	3
—	$R_{\theta JC}$	Thermal resistance, junction to case	—	11	10	°C/W	4
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	—	2	2	°C/W	5

1. Package Your Way
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
3. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
4. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
5. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	 20	 —	 ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

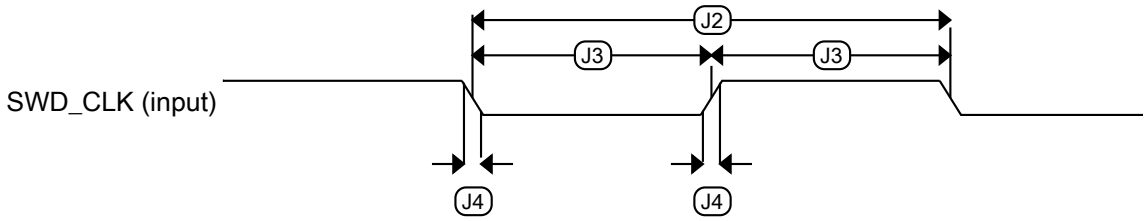


Figure 3. Serial wire clock input timing

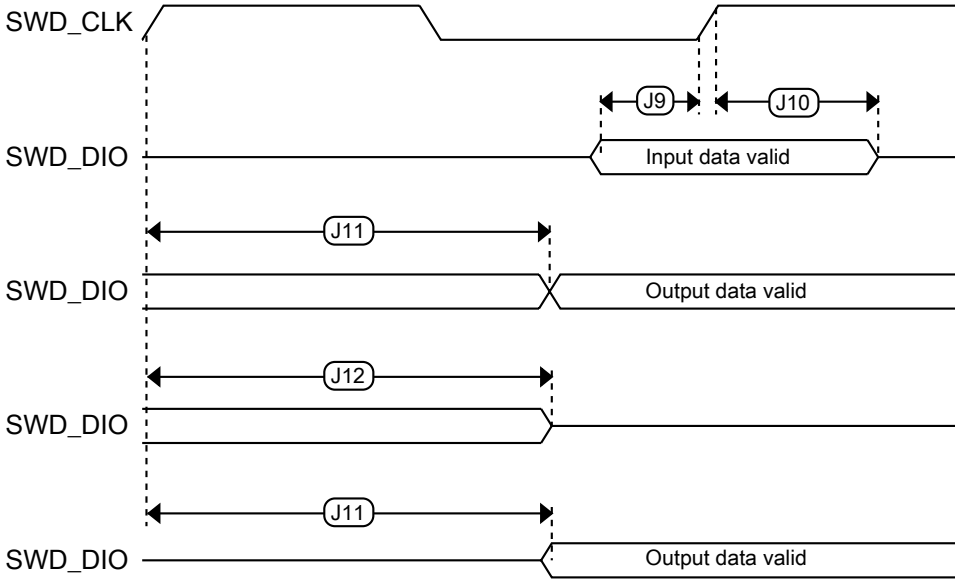


Figure 4. Serial wire data timing

3.1.2 Debug trace timing specifications

Table 14. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	1.5	ns
T_h	Data hold	2	1.0	ns

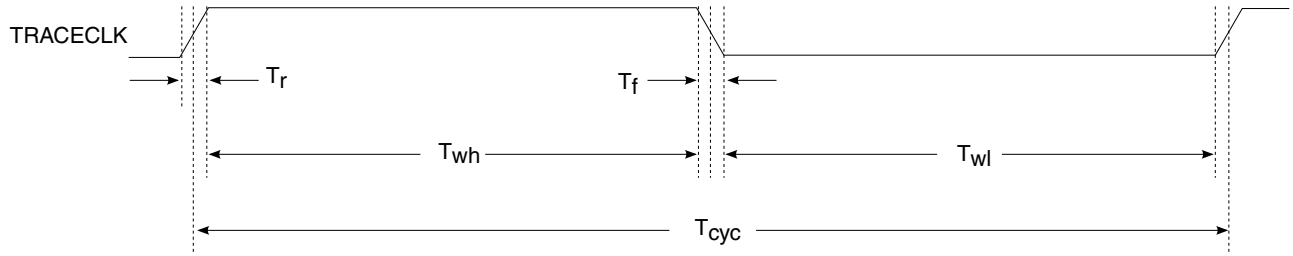


Figure 5. TRACE_CLKOUT specifications

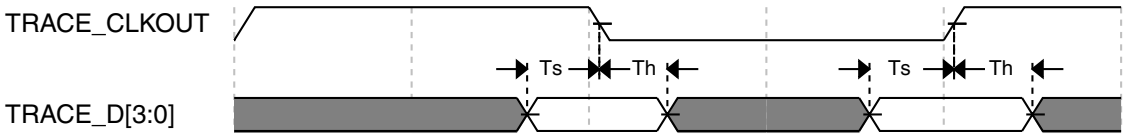


Figure 6. Trace data specifications

3.1.3 JTAG electricals

Table 15. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 15. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 16. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

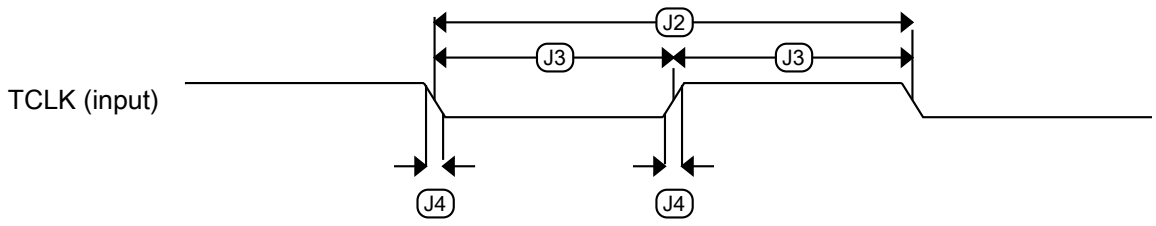


Figure 7. Test clock input timing

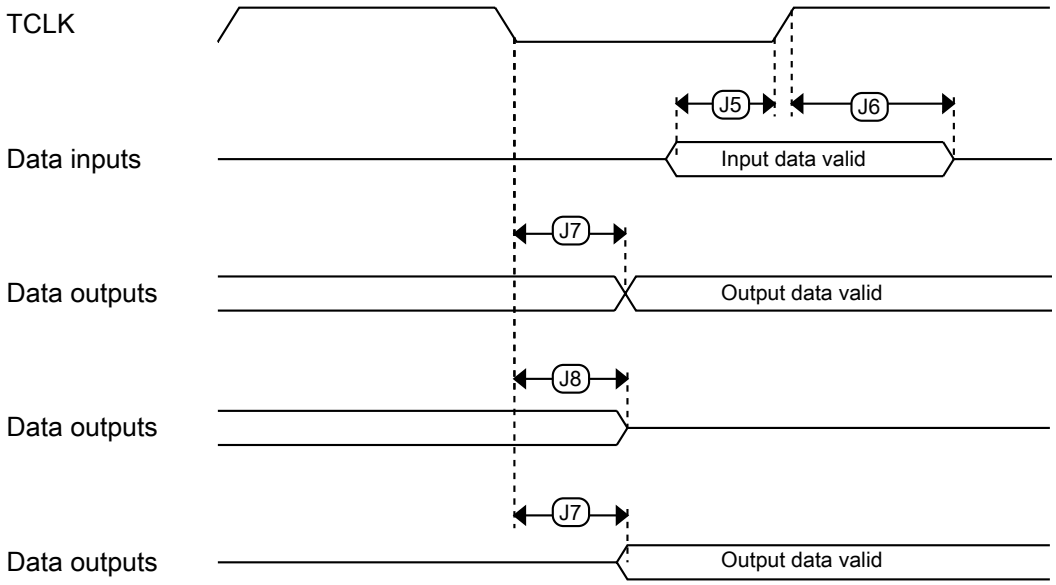


Figure 8. Boundary scan (JTAG) timing

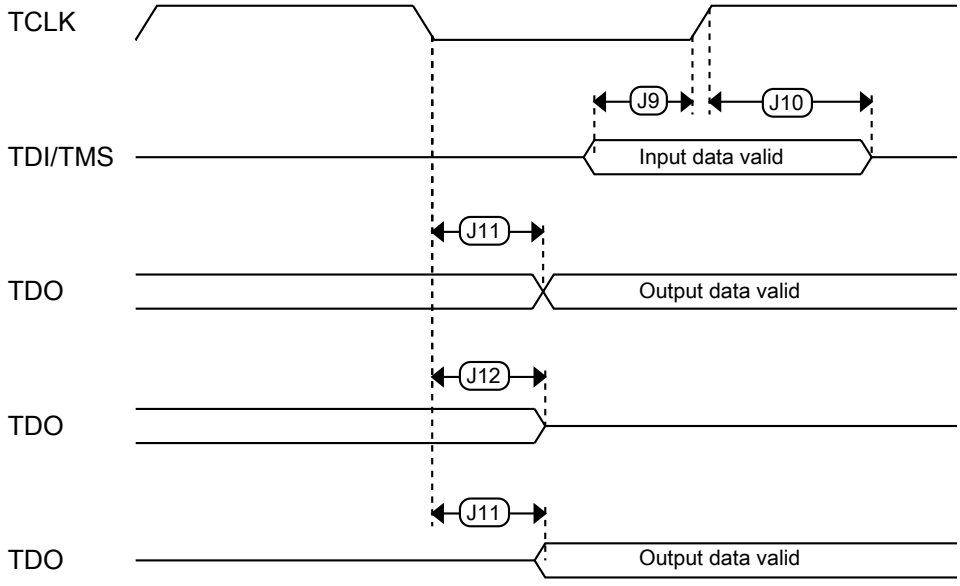


Figure 9. Test Access Port timing

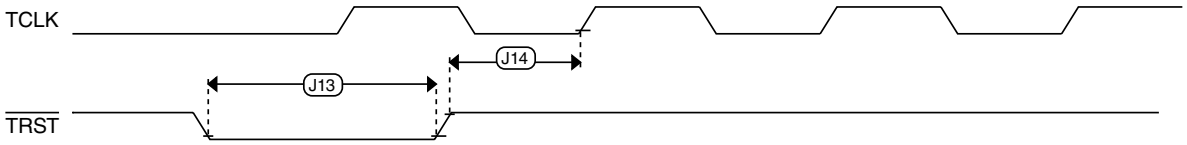


Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 17. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	$\%f_{dco}$	1,
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—		± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f_{ints_t}	—	—	kHz	

Table continues on the next page...

Table 17. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		220	—	480	MHz	
f_{vcoclk}	PLL output frequency		110	—	240	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		110	—	240	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)		—	2.8	—	mA	7
I_{pll}	PLL operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	4.7	—	mA	7
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	120 75	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)						8

Table continues on the next page...

Table 17. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz	—	1350	—	ps	
	• f_{vco} = 120 MHz	—	600	—	ps	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9
F_MCGOUT	Device Clock Frequency • using internal RC oscillator • using external clock source	0.04 0	100 240	MHz		

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz	— —	 500	 —	 nA	1

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	400	—	µA	
	• 8 MHz	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

NOTE

All flash programerase functions can only be performed when the MCU is in Normal Run mode. Programming or erasing the flash in HSRUN mode is not allowed.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversall1m}$	Erase All Blocks high-voltage time for 1 MB	—	832	7232	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec8k}$	Read 1s Section execution time (8 KB flash)	—	—	200	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	870	7400	ms	2

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 24. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	11.8	ns	
FB3	Address, data, and control output hold	1.0	—	ns	1

Table continues on the next page...

Table 24. Flexbus limited voltage range switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB4	Data and FB_TA input setup	11.9	—	ns	
FB5	Data and FB_TA input hold	0.0	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 25. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	12.6	ns	
FB3	Address, data, and control output hold	1.0	—	ns	1
FB4	Data and FB_TA input setup	12.5	—	ns	
FB5	Data and FB_TA input hold	0	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

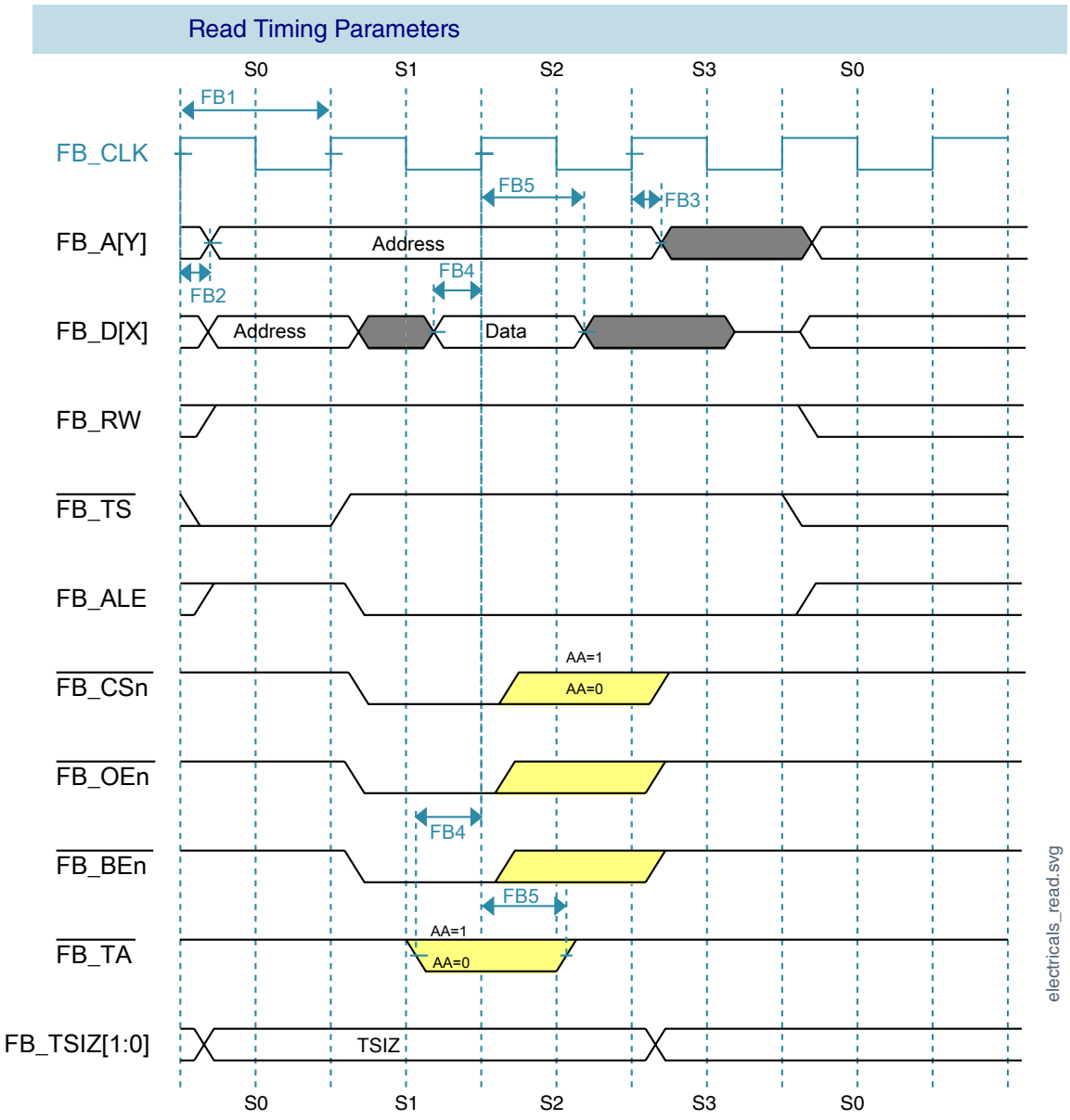


Figure 11. FlexBus read timing diagram

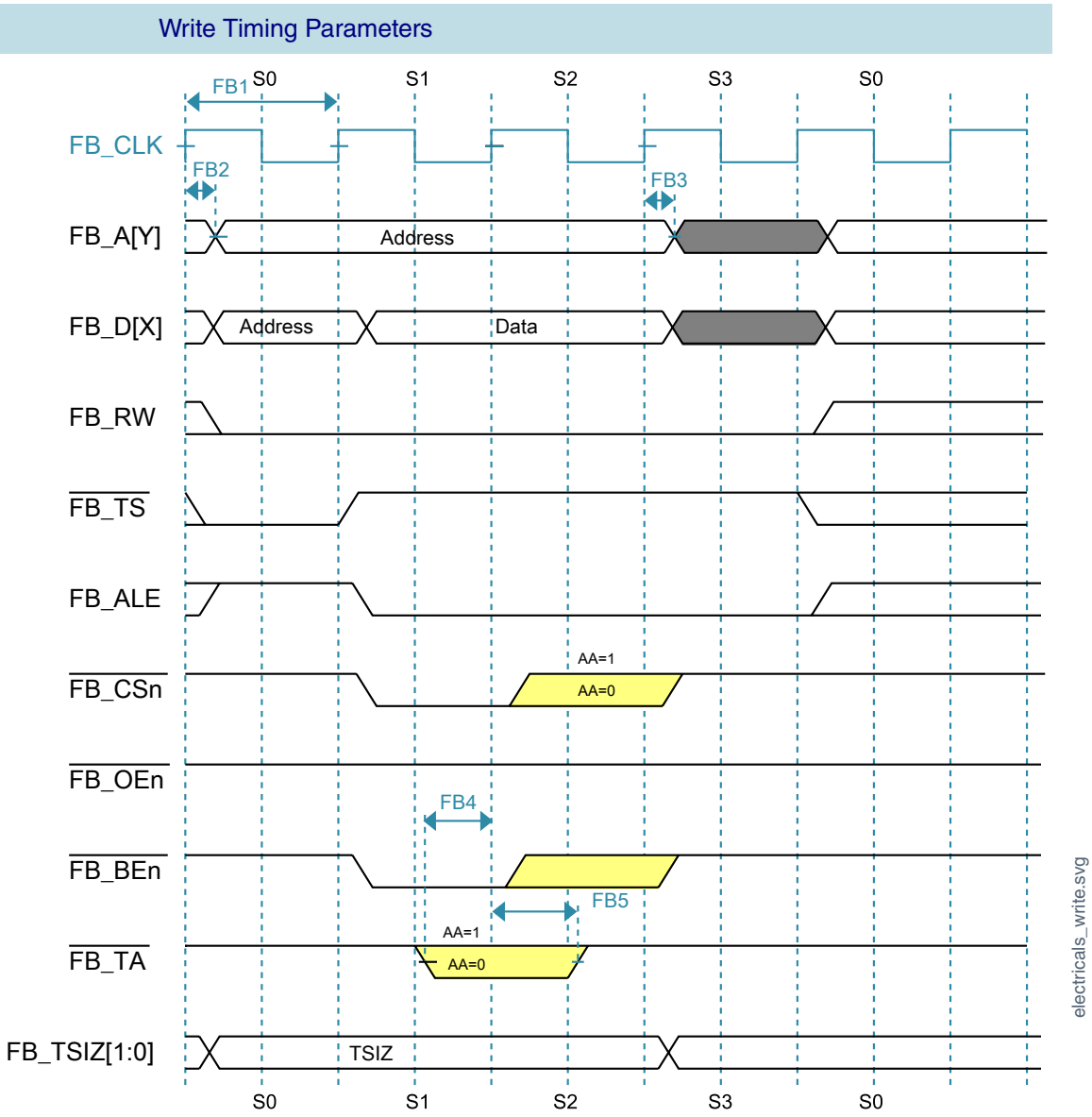


Figure 12. FlexBus write timing diagram

3.6 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.7 Analog

3.7.1 12-bit SAR High Speed Analog-to-Digital Converter (HSADC) parameters

Table 26. 12-bit HSADC electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Analog supply voltage	V_{DDA}	1.71	—	3.6	V
V_{refh} Supply Voltage • $V_{DDA} \geq 2V$ • $V_{DDA} < 2V$	V_{refh}	 2.0 V_{DDA}	V_{DDA}	V_{DDA}	V
V_{refl} Supply Voltage	V_{refl}	V_{SSA}	V_{SSA}	0.1	V
Analog Input					
Full-scale input range (single-ended mode)		V_{refl}		V_{refh}	V
Full-scale input range (differential mode)		$2*(V_{refh} - V_{refl})$			V
Input signal common mode (only for differential mode)		$(V_{refh} + V_{refl})/2$			V
Input sampling capacitance (no parasitic capacitances included)	C_s		5		pF
Current Consumption					
Fs=5MSPS (Conversion in progress, differential mode)[1] • I_{DDA} • I_{DD}		 — —	 1150 85	 — —	µA
Fs=1MSPS (Conversion in progress, differential mode)[1] • I_{DDA} • I_{DD}		 — —	 260 19	 — —	µA
Fs=10kSPS (Conversion in progress, differential mode)[1] • I_{DDA} • I_{DD}		 — —	 19 2.9	 — —	µA
Fs=5MSPS (Conversion in progress, single-ended mode)[1] • I_{DDA} • I_{DD}		 — —	 1030 85	 — —	µA
Fs=1MSPS (Conversion in progress, single-ended mode)[1] • I_{DDA} • I_{DD}		 — —	 230 18	 — —	µA
Fs=10kSPS (Conversion in progress, single-ended mode)[1]					µA

Table continues on the next page...

Table 26. 12-bit HSADC electrical specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
• I_{DDA}		—	19	—	
• I_{DD}		—	2.9	—	
Fs=5MSPS (Conversion not in progress)					µA
• I_{DDA}		—	38	—	
• I_{DD}		—	57	—	
Fs=1MSPS (Conversion not in progress)					µA
• I_{DDA}		—	22	—	
• I_{DD}		—	14	—	
Fs=10kSPS (Conversion not in progress)					µA
• I_{DDA}		—	19	—	
• I_{DD}		—	2.7	—	
Timing Characteristics					
Input clock frequency	f_{clk}	0.14	70	80	MHz
Input clock frequency during calibration	f_{clk}	0.14	—	60	MHz
Sampling rate[2]	F_s				MSPS
• ADCRES=11 (12 bits conversion result)		0.01	5	5.71	
• ADCRES=10 (10 bits conversion result)		0.012	5.83	6.66	
• ADCRES=01 (8 bits conversion result)		0.014	7	8	
• ADCRES=00 (6 bits conversion result)		0.0175	8.75	10	
Conversion cycle[2] (back to back)					Clock cycles
• ADCRES=11 (12 bits conversion result)		14			
• ADCRES=10 (10 bits conversion result)		12			
• ADCRES=01 (8 bits conversion result)		10			
• ADCRES=00 (6 bits conversion result)		8			
Data latency[2]					Clock cycles
• ADCRES=11 (12 bits conversion result)			12.5		
• ADCRES=10 (10 bits conversion result)			10.5		
• ADCRES=01 (8 bits conversion result)			8.5		
• ADCRES=00 (6 bits conversion result)			6.5		
Accuracy (DC or Absolute)					
Integral non-Linearity	INL			+/- 3.0	LSB
Differential non-Linearity	DNL			+/- 1.0	LSB

Table continues on the next page...

Table 26. 12-bit HSADC electrical specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Signal-to-noise and distortion ratio[3]	SINAD		65		dBFS
Offset error (calibration enabled)				+/- 2.0	LSB
Offset error (calibration disabled)				+/- 64	LSB
Total unadjusted error (calibration enabled)	TUE			+/- 5	LSB

1. Successive conversion mode
2. "ADCRES" refers to the resolution selection control signal
3. Value measured with a –0.5dBFS input signal and then extrapolated to full scale.

Table 27. HSADC Input Resolution Table

			Typical			Worst Case		
Input Channels	Resolution	Rin (k)	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles
CHN 0 - 5	12-bit	0.02	9	0	2	20	1	3
		0.07	11	0	2	23	1	3
		0.17	17	0	2	29	1	3
		0.47	34	2	4	46	3	5
		0.97	62	4	6	77	5	7
		4.97	288	22	24	368	28	30
		9.97	576	45	47	840	66	68
		19.97	1179	93	95	1490	118	120
		49.97	3139	250	252	3240	258	260
		99.97	7679	613	615	6199	495	497
	10-bit	0.02	7	0	2	16	0	2
		0.07	9	0	2	18	0	2
		0.17	14	0	2	23	1	3
		0.47	28	1	3	37	2	4
		0.97	51	3	5	63	4	6
		4.97	239	18	20	274	21	23
		9.97	475	37	39	552	43	45
		19.97	949	75	77	1177	93	95
		49.97	2409	192	194	3240	258	260
		99.97	4919	393	395	6199	495	497
	8-bit	0.02	6	0	2	12	0	2
		0.07	8	0	2	14	0	2
		0.17	11	0	2	18	0	2
		0.47	23	1	3	30	1	3

Table continues on the next page...

Table 27. HSADC Input Resolution Table (continued)

			Typical			Worst Case		
Input Channels	Resolution	Rin (k)	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles
		0.97	41	2	4	50	3	5
		4.97	192	14	16	216	16	18
		9.97	380	29	31	425	66	68
		19.97	758	60	62	852	67	69
		49.97	1909	152	154	2209	176	178
		99.97	3819	305	307	4875	389	391
	6-bit	0.02	4	0	2	9	0	2
		0.07	6	0	2	10	0	2
		0.17	9	0	2	13	0	2
		0.47	17	0	2	23	1	3
		0.97	31	1	3	38	2	4
		4.97	144	11	13	162	12	14
		9.97	286	22	24	318	24	26
		19.97	571	45	47	630	49	51
		49.97	1429	113	115	1579	125	127
		99.97	2859	228	230	3189	254	256
All other channels	12-bit	0.1	41	2	4	75	5	7
		0.6	69	5	7	114	8	10
		4.6	296	23	25	494	39	41
		9.6	584	46	48	919	73	75
		19.6	1189	94	96	1669	133	135
		49.6	3169	253	255	3589	286	288
		99.6	7689	614	616	6869	549	551
	10-bit	0.1	34	2	4	59	4	6
		0.6	57	4	6	89	6	8
		4.6	244	19	21	331	25	27
		9.6	480	37	39	665	52	54
		19.6	953	75	77	1669	133	135
		49.6	2409	192	194	3589	286	288
		99.6	4929	393	395	6869	549	551
	8-bit	0.1	27	1	3	47	3	5
		0.6	46	3	5	70	5	7
		4.6	196	15	17	255	19	21
		9.6	384	30	32	491	38	40

Table continues on the next page...

Table 27. HSADC Input Resolution Table (continued)

			Typical			Worst Case		
Input Channels	Resolution	Rin (k)	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles	Min Sampling Time (ns)	Additional clk cycles (SAMPT_x)	Total Cycles
		19.6	761	60	62	977	77	79
		49.6	1909	152	154	2619	209	211
		99.6	3819	305	307	6869	549	551
	6-bit	0.1	21	1	3	36	2	4
		0.6	35	2	4	53	3	5
		4.6	148	11	13	191	14	16
		9.6	290	22	24	365	28	30
		19.6	573	45	47	714	56	58
		49.6	1439	114	116	1789	142	144
		99.6	2859	228	230	3629	289	291

3.7.2 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 1 and Table 29 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.7.2.1 16-bit ADC operating conditions

Table 28. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	

Table continues on the next page...

Table 28. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

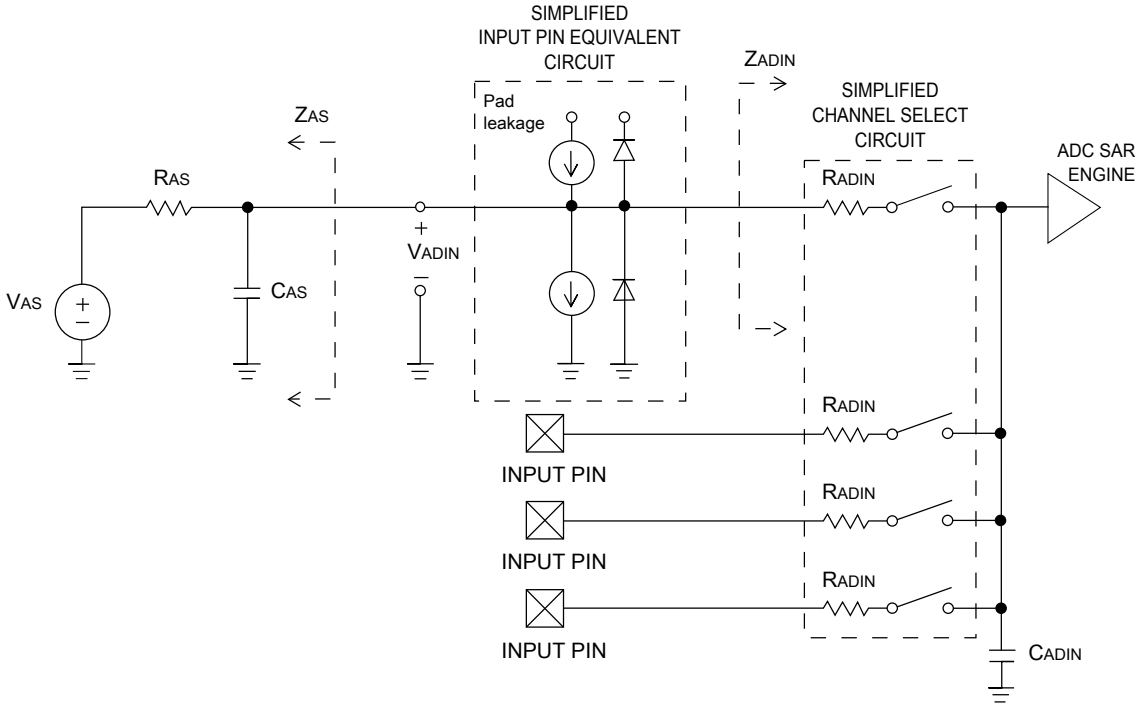


Figure 13. ADC input impedance equivalency diagram

3.7.2.2 16-bit ADC electrical characteristics

Table 29. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 29. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes	—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — — 	dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

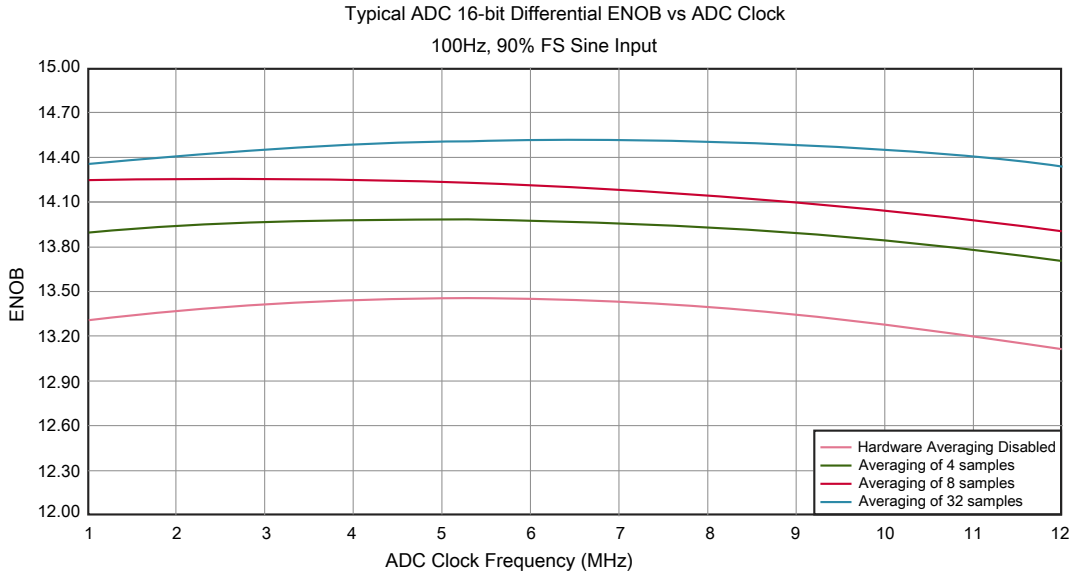


Figure 14. Typical ENOB vs. ADC_CLK for 16-bit differential mode

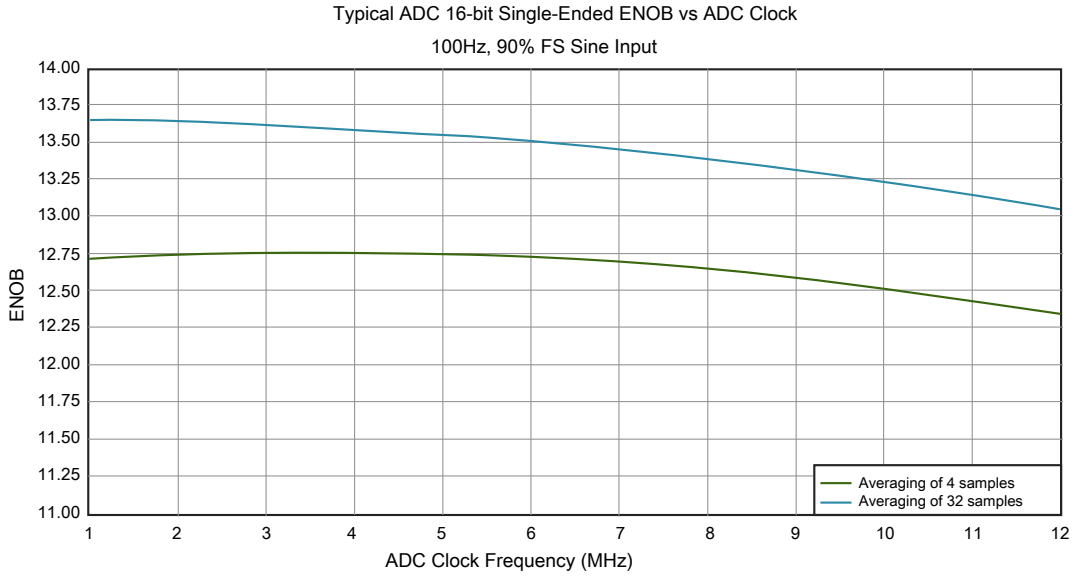


Figure 15. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.7.3 CMP and 6-bit DAC electrical specifications

Table 30. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

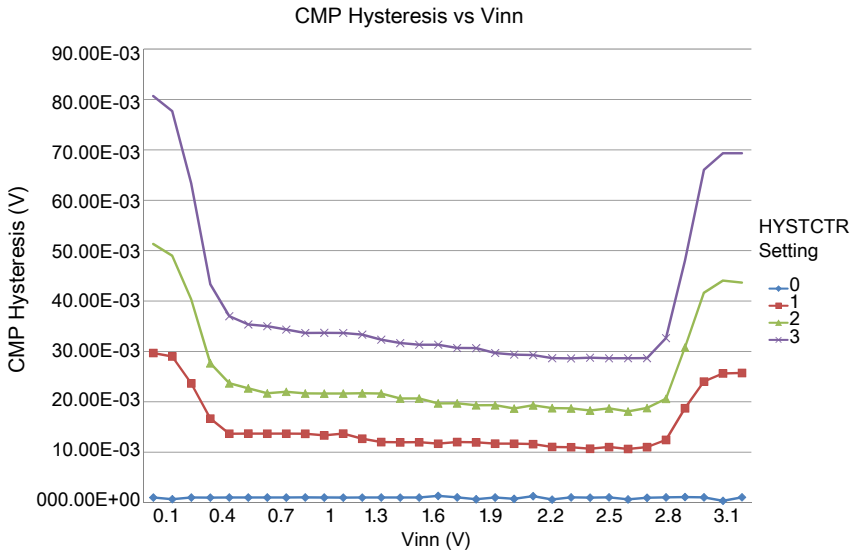


Figure 16. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

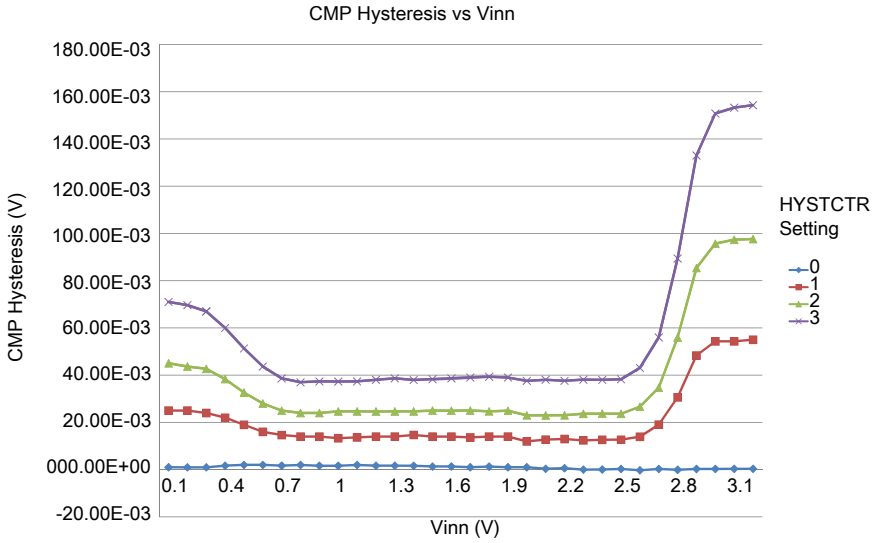


Figure 17. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.7.4 12-bit DAC electrical characteristics

3.7.4.1 12-bit DAC operating requirements

Table 31. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.7.4.2 12-bit DAC operating behaviors

Table 32. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) • High-speed mode • Low speed mode	—	1	5	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} –100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	

Table continues on the next page...

Table 32. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

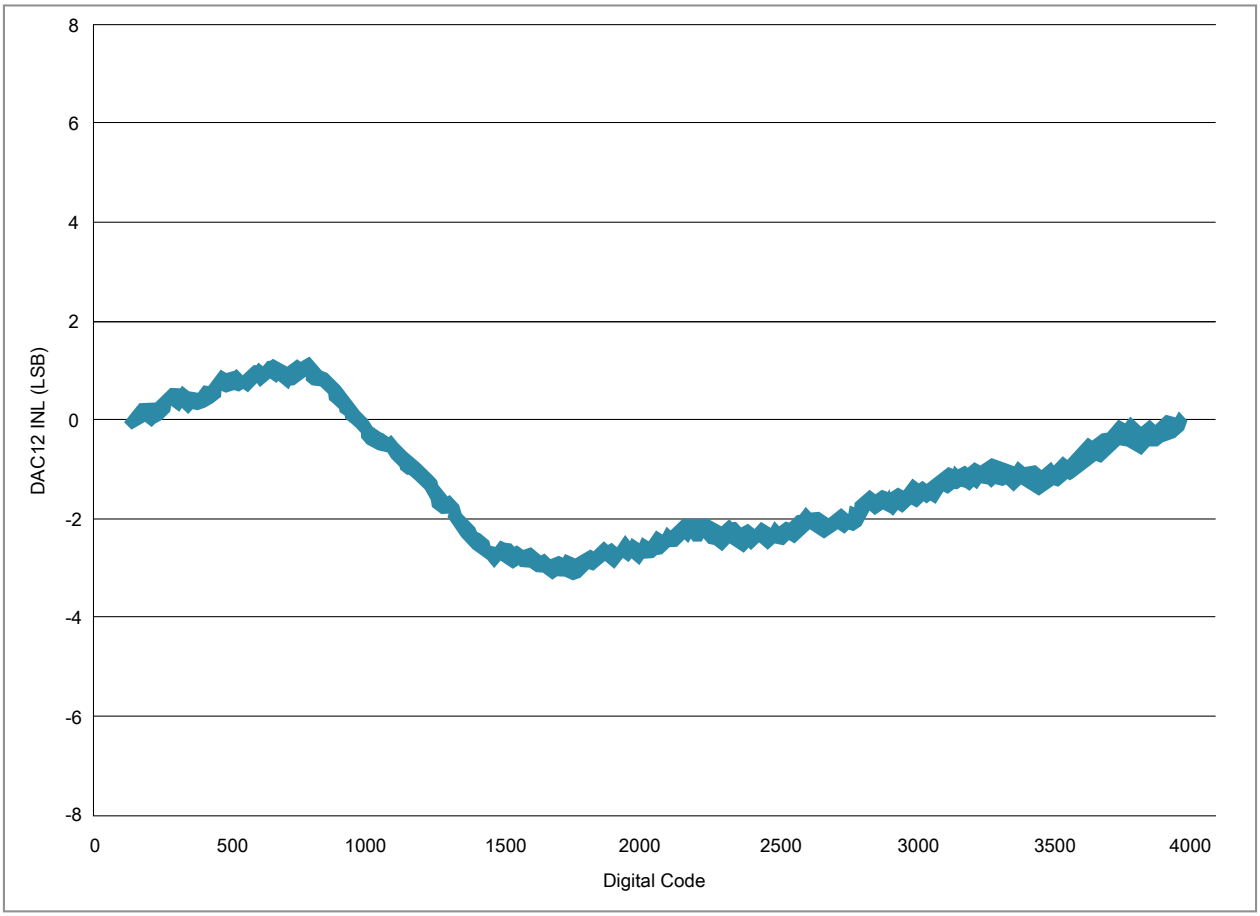


Figure 18. Typical INL error vs. digital code

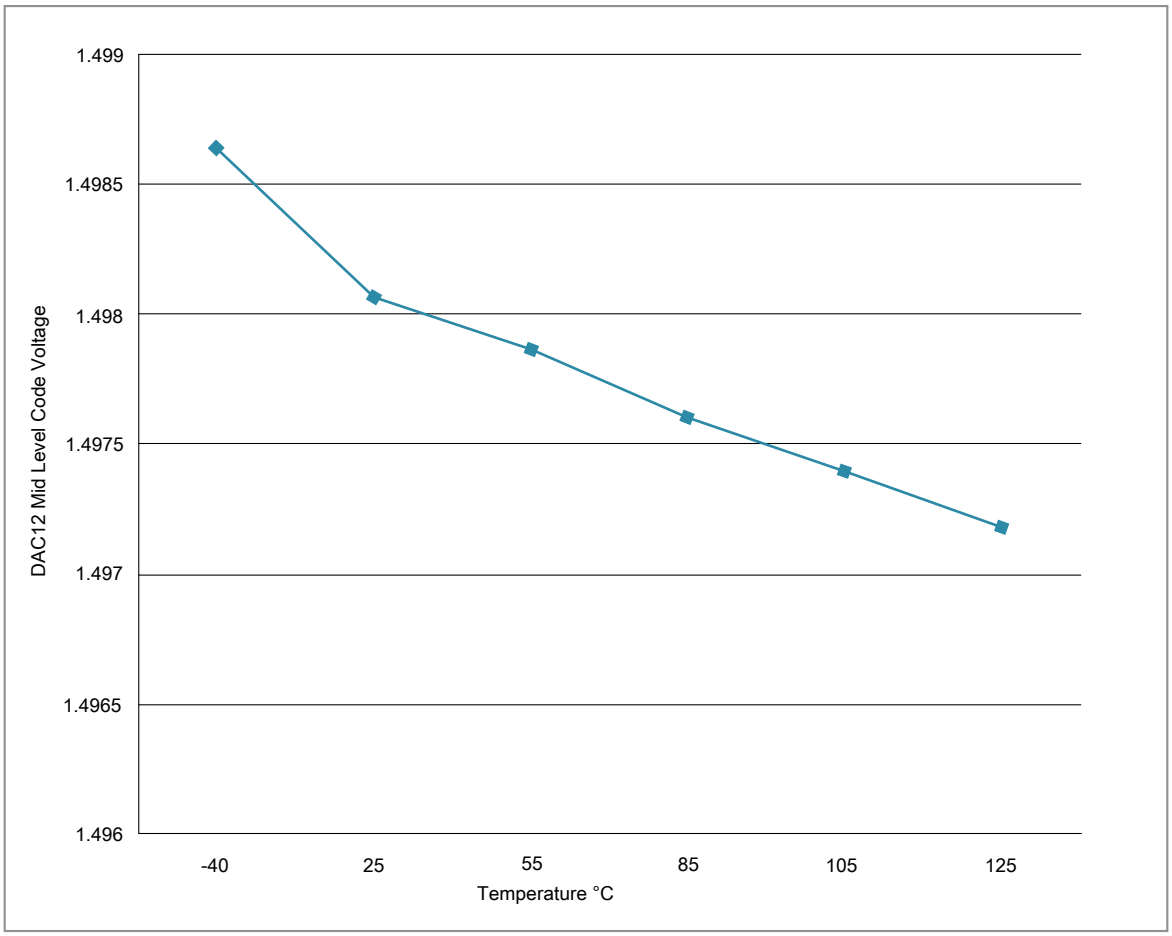


Figure 19. Offset at half scale vs. temperature

3.8 Timers

See General switching specifications.

3.8.1 Enhanced NanoEdge PWM characteristics

Table 33. NanoEdge PWM timing parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency		80		120	MHz
NanoEdge Placement (NEP) Step Size[1] • @ 80 MHz • @ 120 MHz	pwmp	 — —	 390 260	 — —	ps
Power-up Time[2]	t_{pu}		25		µs

1. Temperature and voltage variations do not affect NanoEdge Placement step size.
2. Powerdown to NanoEdge mode transition.

3.9 Communication interfaces

3.9.1 CAN switching specifications

See General switching specifications.

3.9.2 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.9.2.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 34. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	Operating Voltage	1.71	3.6	V
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

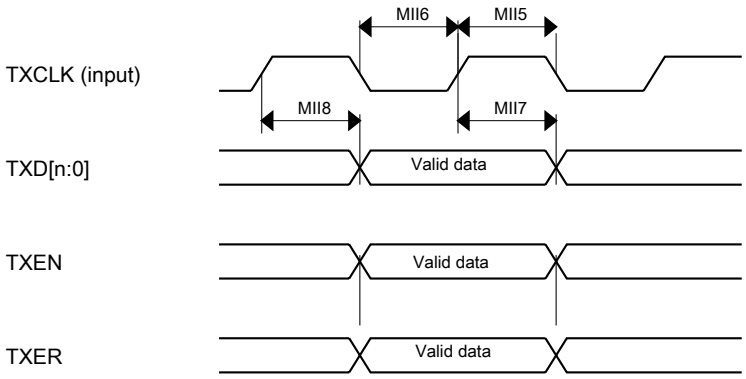


Figure 20. RMII/MII transmit signal timing diagram

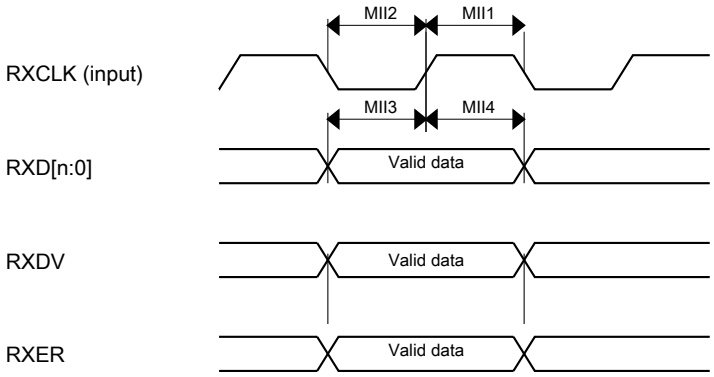


Figure 21. RMII/MII receive signal timing diagram

3.9.2.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 35. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	Operating Voltage	1.71	3.6	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 35. RMII signal switching specifications (continued)

Num	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15.4	ns

3.9.3 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 36. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* to DSPI_SCK output valid	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* output hold	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

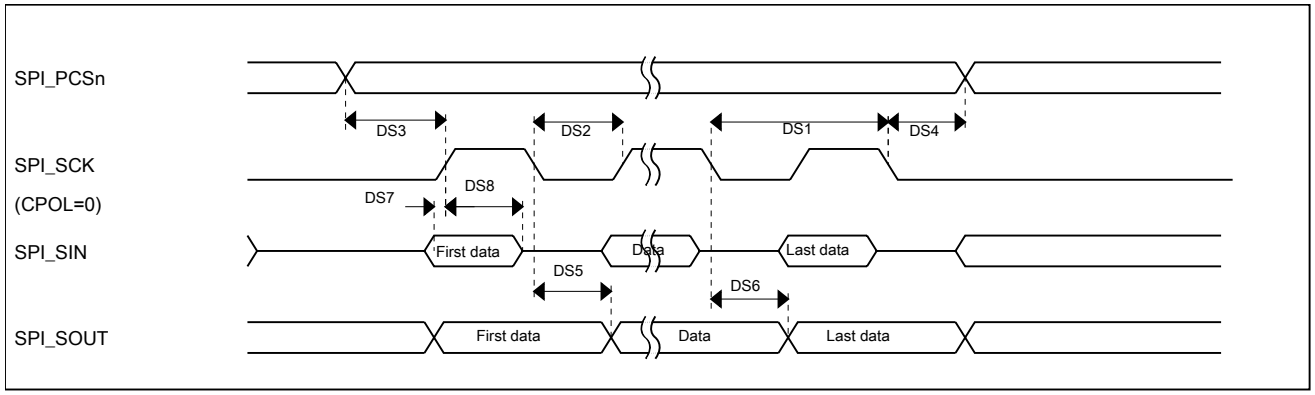


Figure 22. DSPI classic SPI timing — master mode

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

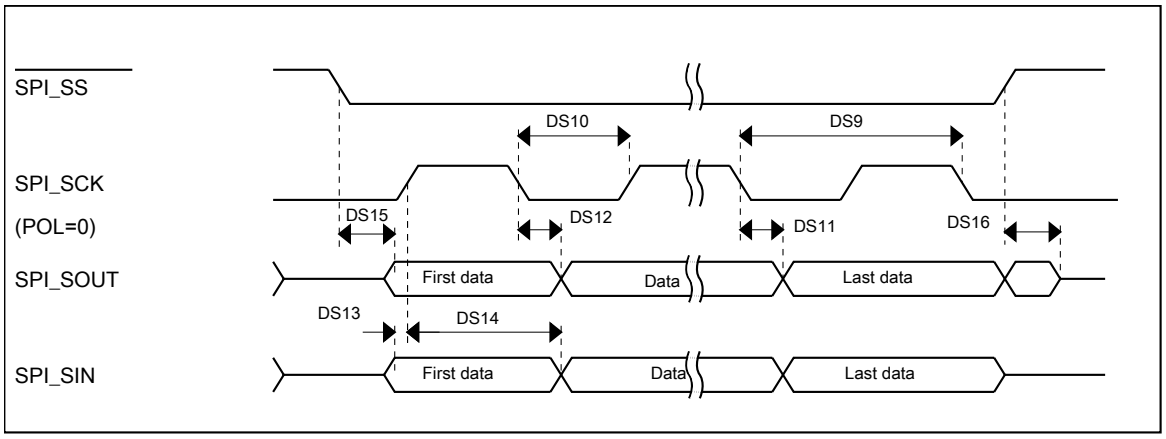


Figure 23. DSPI classic SPI timing — slave mode

3.9.4 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

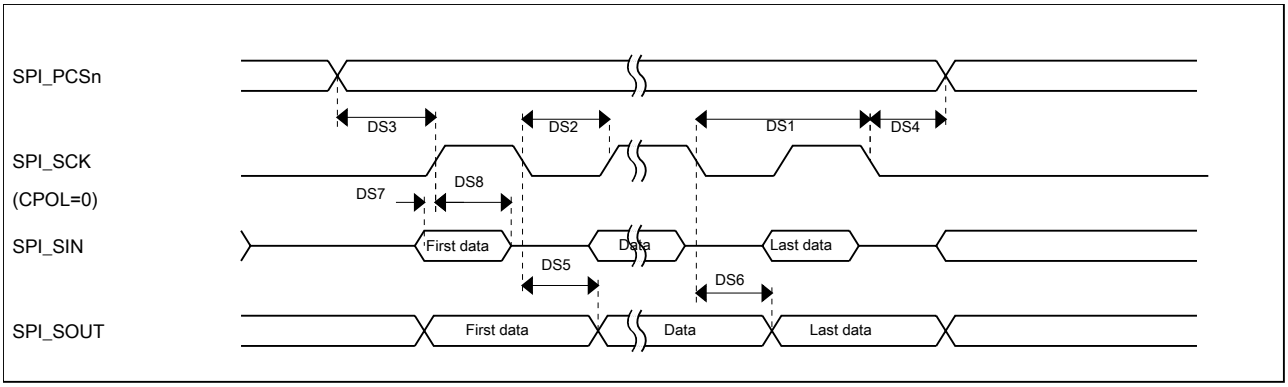


Figure 24. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 39. Slave mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
	Frequency of operation	—	12.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	27.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

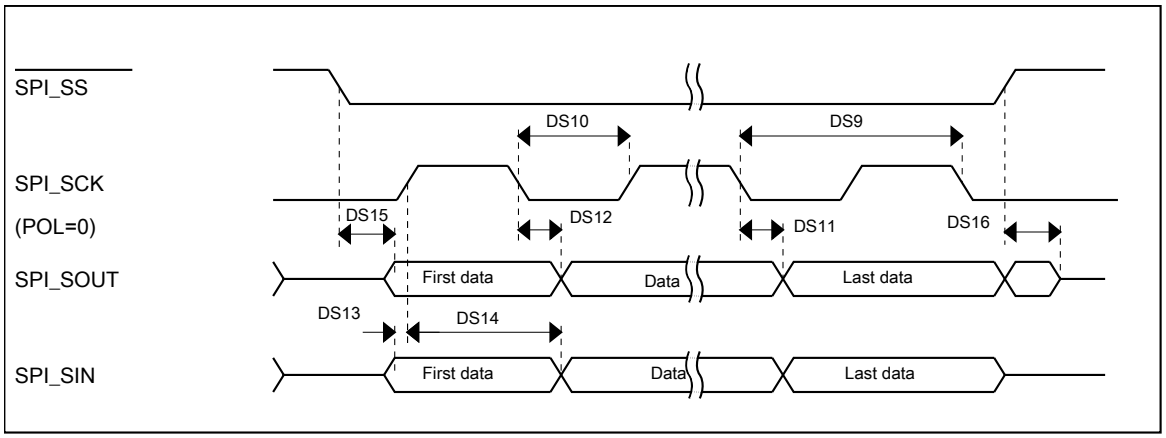


Figure 25. DSPI classic SPI timing — slave mode

3.9.5 I²C

See General switching specifications.

3.9.6 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin MAPBGA	98ASA00222D
144-pin LQFP	98ASS23177W
100-pin LQFP	98ASS23308W

5 Pinouts and Packaging

5.1 KV5x Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
D3	1	1	PTE0	HSADC0B_CH16/ HSADC1A_CH0	HSADC0B_CH16/ HSADC1A_CH0	PTE0	SPI1_ PCS1	UART1_ TX	XB_ OUT10	XB_IN11	I2C1_SDA		TRACE_ CLKOUT	
D2	2	2	PTE1/ LLWU_P0	HSADC0B_CH17/ HSADC1A_CH1	HSADC0B_CH17/ HSADC1A_CH1	PTE1/ LLWU_P0	SPI1_ SOUT	UART1_ RX	XB_ OUT11	XB_IN7	I2C1_SCL		TRACE_ D3	
D1	3	3	PTE2/ LLWU_P1	HSADC0B_CH10/ HSADC1B_CH0	HSADC0B_CH10/ HSADC1B_CH0	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b					TRACE_ D2	
E4	4	4	PTE3	HSADC0B_CH11/ HSADC1B_CH1	HSADC0B_CH11/ HSADC1B_CH1	PTE3	SPI1_SIN	UART1_ RTS_b					TRACE_ D1	
E5	5	—	VDD	VDD	VDD									
F6	6	—	VSS	VSS	VSS									
E3	7	5	PTE4/ LLWU_P2	HSADC1A_CH4/ ADC0_	HSADC1A_CH4/ ADC0_	PTE4/ LLWU_P2	SPI1_ PCS0	UART3_ TX					TRACE_ D0	

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
				SE2/ ADC0_ DP2	SE2/ ADC0_ DP2									
E2	8	6	PTE5	HSADC1A _CH5/ ADC0_ SE10/ ADC0_ DM2	HSADC1A _CH5/ ADC0_ SE10/ ADC0_ DM2	PTE5	SPI1_ PCS2	UART3_ RX		eflexPWM 1_A0	FTM3_ CH0			
E1	9	7	PTE6/ LLWU_ P16	HSADC1B _CH7/ ADC0_ SE4a	HSADC1B _CH7/ ADC0_ SE4a	PTE6/ LLWU_ P16	SPI1_ PCS3	UART3_ CTS_b		eflexPWM 1_B0	FTM3_ CH1			
F4	10	—	PTE7	DISABLED		PTE7		UART3_ RTS_b		eflexPWM 1_A1	FTM3_ CH2			
F3	11	—	PTE8	DISABLED		PTE8		UART5_ TX		eflexPWM 1_B1	FTM3_ CH3			
F2	12	—	PTE9/ LLWU_ P17	DISABLED		PTE9/ LLWU_ P17		UART5_ RX		eflexPWM 1_A2	FTM3_ CH4			
F1	13	—	PTE10/ LLWU_ P18	DISABLED		PTE10/ LLWU_ P18		UART5_ CTS_b		eflexPWM 1_B2	FTM3_ CH5			
G4	14	—	PTE11	HSADC1A _CH6/ ADC0_ SE3/ ADC0_ DP3	HSADC1A _CH6/ ADC0_ SE3/ ADC0_ DP3	PTE11		UART5_ RTS_b		eflexPWM 1_A3	FTM3_ CH6			
G3	15	—	PTE12	HSADC1B _CH6/ ADC0_ SE11/ ADC0_ DM3	HSADC1B _CH6/ ADC0_ SE11/ ADC0_ DM3	PTE12				eflexPWM 1_B3	FTM3_ CH7			
E6	16	8	VDD	VDD	VDD									
F7	17	9	VSS	VSS	VSS									
H1	18	10	PTE16	HSADC0A _CH0/ ADC0_ SE1/ ADC0_ DP1	HSADC0A _CH0/ ADC0_ SE1/ ADC0_ DP1	PTE16	SPI0_ PCS0	UART2_ TX	FTM_ CLKIN0		FTM0_ FLT3			
H2	19	11	PTE17/ LLWU_ P19	HSADC0A _CH1/ ADC0_ SE9/ ADC0_ DM1	HSADC0A _CH1/ ADC0_ SE9/ ADC0_ DM1	PTE17/ LLWU_ P19	SPI0_SCK	UART2_ RX	FTM_ CLKIN1		LPTMR0_ ALT3			

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
G1	20	12	PTE18/ LLWU_ P20	HSADC0B _CH0/ ADC0_ SE5a	HSADC0B _CH0/ ADC0_ SE5a	PTE18/ LLWU_ P20	SPI0_ SOUT	UART2_ CTS_b	I2C0_SDA					
G2	21	13	PTE19	HSADC0B _CH1/ ADC0_ SE6a	HSADC0B _CH1/ ADC0_ SE6a	PTE19	SPI0_SIN	UART2_ RTS_b	I2C0_SCL		CMP3_ OUT			
H3	22	—	VSS	VSS	VSS									
J1	23	14	HSADC0A _CH6	HSADC0A _CH6/ ADC0_ SE7a	HSADC0A _CH6/ ADC0_ SE7a									
J2	24	15	HSADC0A _CH7/ ADC0_ SE4b	HSADC0A _CH7/ ADC0_ SE4b	HSADC0A _CH7/ ADC0_ SE4b									
K1	25	16	PTE20	HSADC0A _CH8/ ADC0_ SE5b	HSADC0A _CH8/ ADC0_ SE5b	PTE20		FTM1_ CH0	UART0_ TX	FTM1_ QD_PHA				
K2	26	17	PTE21	HSADC0A _CH9/ HSADC1A _CH7	HSADC0A _CH9/ HSADC1A _CH7	PTE21	XB_IN9	FTM1_ CH1	UART0_ RX	FTM1_ QD_PHB				
L1	27	18	HSADC0A _CH2/ HSADC1A _CH2	HSADC0A _CH2/ HSADC1A _CH2	HSADC0A _CH2/ HSADC1A _CH2									
L2	28	19	HSADC0A _CH3/ HSADC1A _CH3	HSADC0A _CH3/ HSADC1A _CH3	HSADC0A _CH3/ HSADC1A _CH3									
M1	29	20	HSADC0A _CH10/ HSADC1B _CH2	HSADC0A _CH10/ HSADC1B _CH2	HSADC0A _CH10/ HSADC1B _CH2									
M2	30	21	HSADC0A _CH11/ HSADC1B _CH3	HSADC0A _CH11/ HSADC1B _CH3	HSADC0A _CH11/ HSADC1B _CH3									
H5	31	22	VDDA	VDDA	VDDA									
G5	32	23	VREFH	VREFH	VREFH									
G6	33	24	VREFL	VREFL	VREFL									
H6	34	25	VSSA	VSSA	VSSA									
K3	35	—	ADC0_ SE0/ ADC0_	ADC0_ SE0/ ADC0_	ADC0_ SE0/ ADC0_									

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
			DP0/ CMP2_IN5	DP0/ CMP2_IN5	DP0/ CMP2_IN5									
J3	36	—	ADC0_ SE8/ ADC0_ DM0/ CMP1_IN2	ADC0_ SE8/ ADC0_ DM0/ CMP1_IN2	ADC0_ SE8/ ADC0_ DM0/ CMP1_IN2									
M3	37	26	PTE29	HSADC0A _CH4/ CMP1_ IN5/ CMP0_IN5	HSADC0A _CH4/ CMP1_ IN5/ CMP0_IN5	PTE29		FTM0_ CH2		FTM_ CLKIN0				
L3	38	27	PTE30	DAC0_ OUT/ CMP1_ IN3/ HSADC0A _CH5	DAC0_ OUT/ CMP1_ IN3/ HSADC0A _CH5	PTE30		FTM0_ CH3		FTM_ CLKIN1				
L4	39	28	HSADC0A _CH12/ CMP0_ IN4/ CMP2_IN3	HSADC0A _CH12/ CMP0_ IN4/ CMP2_IN3	HSADC0A _CH12/ CMP0_ IN4/ CMP2_IN3									
L5	40	—	PTE13	DISABLED		PTE13								
M7	41	—	PTE22	DISABLED		PTE22		FTM2_ CH0	XB_IN2	FTM2_ QD_PHA				
M6	42	—	PTE23	DISABLED		PTE23		FTM2_ CH1	XB_IN3	FTM2_ QD_PHB				
—	—	29	VSS	VSS	VSS									
L6	43	30	VDD	VDD	VDD									
—	44	—	VSS	VSS	VSS									
M4	45	31	PTE24	HSADC0B _CH4/ HSADC1B _CH4	HSADC0B _CH4/ HSADC1B _CH4	PTE24	CAN1_TX	FTM0_ CH0	XB_IN2	I2C0_SCL	EWM_ OUT_b	XB_OUT4	UART4_ TX	
K5	46	32	PTE25/ LLWU_ P21	HSADC0B _CH5/ HSADC1B _CH5	HSADC0B _CH5/ HSADC1B _CH5	PTE25/ LLWU_ P21	CAN1_RX	FTM0_ CH1	XB_IN3	I2C0_SDA	EWM_IN	XB_OUT5	UART4_ RX	
K4	47	33	PTE26	DISABLED		PTE26	ENET_ 1588_ CLKIN	FTM0_ CH4					UART4_ CTS_b	
J4	48	—	PTE27	DISABLED		PTE27	CAN2_TX						UART4_ RTS_b	
H4	49	—	PTE28	DISABLED		PTE28	CAN2_RX							
J5	50	34	PTA0	JTAG_ TCLK/ SWD_CLK		PTA0	UART0_ CTS_b/	FTM0_ CH5	XB_IN4	EWM_IN		JTAG_ TCLK/ SWD_CLK		

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
							UART0_ COL_b							
J6	51	35	PTA1	JTAG_TDI		PTA1	UART0_ RX	FTM0_ CH6	CMP0_ OUT	FTM2_ QD_PHA	FTM1_ CH1	JTAG_TDI		
K6	52	36	PTA2	JTAG_ TDO/ TRACE_ SWO		PTA2	UART0_ TX	FTM0_ CH7	CMP1_ OUT	FTM2_ QD_PHB	FTM1_ CH0	JTAG_ TDO/ TRACE_ SWO		
K7	53	37	PTA3	JTAG_ TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_ CH0	XB_IN9	EWM_ OUT_b	eflexPWM 0_A0	JTAG_ TMS/ SWD_DIO		
L7	54	38	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		FTM0_ CH1	XB_IN10	FTM0_ FLT3	eflexPWM 0_B0	NMI_b		
M8	55	39	PTA5	DISABLED		PTA5		FTM0_ CH2	RMII0_ RXER/ MII0_ RXER	CMP2_ OUT		JTAG_ TRST_b		
E7	56	40	VDD	VDD	VDD									
G7	57	41	VSS	VSS	VSS									
J7	58	—	PTA6	DISABLED		PTA6		FTM0_ CH3		CLKOUT		TRACE_ CLKOUT		
J8	59	—	PTA7	HSADC1B _CH8	HSADC1B _CH8	PTA7		FTM0_ CH4		RMII0_ MDIO/ MII0_ MDIO		TRACE_ D3		
K8	60	—	PTA8	HSADC1B _CH9	HSADC1B _CH9	PTA8		FTM1_ CH0		RMII0_ MDC/ MII0_MDC		TRACE_ D2		
L8	61	—	PTA9	DISABLED		PTA9		FTM1_ CH1		MII0_ RXD3		TRACE_ D1		
M9	62	—	PTA10/ LLWU_ P22	DISABLED		PTA10/ LLWU_ P22		FTM2_ CH0		MII0_ RXD2	FTM2_ QD_PHA	TRACE_ D0		
L9	63	—	PTA11/ LLWU_ P23	DISABLED		PTA11/ LLWU_ P23		FTM2_ CH1		MII0_ RXCLK	FTM2_ QD_PHB		I2C0_SDA	
K9	64	42	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_ CH0		RMII0_ RXD1/ MII0_ RXD1		FTM1_ QD_PHA	I2C0_SCL	
J9	65	43	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_ CH1		RMII0_ RXD0/ MII0_ RXD0		FTM1_ QD_PHB	I2C1_SDA	
L10	66	44	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_ PCS0	UART0_ TX	CAN2_TX	RMII0_ CRS_DV/ MII0_ RXDV			I2C1_SCL	

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
L11	67	45	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX	CAN2_RX	RMII0_TXEN/ MII0_TXEN				
K10	68	46	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b		RMII0_TXD0/ MII0_TXD0				
K11	69	47	PTA17	HSADC0A_CH15	HSADC0A_CH15	PTA17	SPI0_SIN	UART0_RTS_b		RMII0_TXD1/ MII0_TXD1				
E8	70	48	VDD	VDD	VDD									
G8	71	49	VSS	VSS	VSS									
M12	72	50	PTA18	EXTAL0	EXTAL0	PTA18	XB_IN7	FTM0_FLT2	FTM_CLKIN0	XB_OUT8	FTM3_CH2			
M11	73	51	PTA19	XTAL0	XTAL0	PTA19	XB_IN8	FTM1_FLT0	FTM_CLKIN1	XB_OUT9	LPTMR0_ALT1			
L12	74	52	RESET_b	RESET_b	RESET_b									
K12	75	—	PTA24	DISABLED		PTA24	XB_IN4			MII0_TXD2			FB_A29	
J12	76	—	PTA25	DISABLED		PTA25	XB_IN5			MII0_TXCLK			FB_A28	
J11	77	—	PTA26	DISABLED		PTA26				MII0_TXD3			FB_A27	
J10	78	—	PTA27	DISABLED		PTA27				MII0_CRS			FB_A26	
H12	79	—	PTA28	DISABLED		PTA28				MII0_TXER			FB_A25	
H11	80	—	PTA29	DISABLED		PTA29				MII0_COL			FB_A24	
H10	81	53	PTB0/ LLWU_P5	HSADC0B_CH2	HSADC0B_CH2	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	UART0_RX	RMII0_MDIO/ MII0_MDIO	
H9	82	54	PTB1	HSADC0B_CH3	HSADC0B_CH3	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_PHB	UART0_TX	RMII0_MDC/ MII0_MDC	
G12	83	55	PTB2	HSADC0A_CH14/ CMP2_IN2	HSADC0A_CH14/ CMP2_IN2	PTB2	I2C0_SCL	UART0_RTS_b	FTM0_FLT1	ENET0_1588_TMR0	FTM0_FLT3			
G11	84	56	PTB3	HSADC0B_CH15/ CMP3_IN5	HSADC0B_CH15/ CMP3_IN5	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b		ENET0_1588_TMR1	FTM0_FLT0			
G10	85	—	PTB4	ADC0_SE6b	ADC0_SE6b	PTB4			eflexPWM1_X0	ENET0_1588_TMR2	FTM1_FLT0			
G9	86	—	PTB5	ADC0_SE7b	ADC0_SE7b	PTB5			eflexPWM1_X1	ENET0_1588_TMR3	FTM2_FLT0			

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
F12	87	—	PTB6	HSADC1A_CH12	HSADC1A_CH12	PTB6	CAN2_TX		eflexPWM1_X2				FB_AD23	
F11	88	—	PTB7	HSADC1A_CH13	HSADC1A_CH13	PTB7	CAN2_RX		eflexPWM1_X3				FB_AD22	
F10	89	—	PTB8	DISABLED		PTB8		UART3_RTS_b					FB_AD21	
F9	90	57	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_b		ENET0_1588_TMR2			FB_AD20	
E12	91	58	PTB10	HSADC0B_CH6	HSADC0B_CH6	PTB10	SPI1_PCS0	UART3_RX		ENET0_1588_TMR3	FTM0_FLT1		FB_AD19	
E11	92	59	PTB11	HSADC0B_CH7	HSADC0B_CH7	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		FB_AD18	
H7	93	60	VSS	VSS	VSS									
F5	94	61	VDD	VDD	VDD									
E10	95	62	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN2	CAN0_TX	EWM_IN	XB_IN5	FB_AD17	
E9	96	63	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	CAN0_RX	EWM_OUT_b		FB_AD16	
D12	97	64	PTB18	DISABLED		PTB18	CAN0_TX	FTM2_CH0	FTM3_CH2	eflexPWM1_A1	FTM2_QD_PHA		FB_AD15	
D11	98	65	PTB19	DISABLED		PTB19	CAN0_RX	FTM2_CH1	FTM3_CH3	eflexPWM1_B1	FTM2_QD_PHB		FB_OE_b	
D10	99	66	PTB20	DISABLED		PTB20	SPI2_PCS0			eflexPWM0_X0	CMP0_OUT		FB_AD31	
D9	100	67	PTB21	DISABLED		PTB21	SPI2_SCK			eflexPWM0_X1	CMP1_OUT		FB_AD30	
C12	101	68	PTB22	DISABLED		PTB22	SPI2_SOUT			eflexPWM0_X2	CMP2_OUT		FB_AD29	
C11	102	69	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		eflexPWM0_X3	CMP3_OUT		FB_AD28	
B12	103	70	PTC0	HSADC0B_CH8	HSADC0B_CH8	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0	FB_AD14	
B11	104	71	PTC1/LLWU_P6	HSADC0B_CH9	HSADC0B_CH9	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	eflexPWM0_A3	XB_IN11		FB_AD13	
A12	105	72	PTC2	HSADC1B_CH10/CMP1_IN0	HSADC1B_CH10/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	eflexPWM0_B3	XB_IN6		FB_AD12	
A11	106	73	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0			
H8	107	74	VSS	VSS	VSS									
—	108	75	VDD	VDD	VDD									
A9	109	76	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		FB_AD11	

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
D8	110	77	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XB_IN2		CMP0_ OUT	FTM0_ CH2	FB_AD10	
C8	111	78	PTC6/ LLWU_ P10	CMP2_ IN4/ CMP0_IN0	CMP2_ IN4/ CMP0_IN0	PTC6/ LLWU_ P10	SPI0_ SOUT	PDB0_ EXTRG	XB_IN3	UART0_ RX	XB_OUT6	I2C0_SCL	FB_AD9	
B8	112	79	PTC7	CMP3_ IN4/ CMP0_IN1	CMP3_ IN4/ CMP0_IN1	PTC7	SPI0_SIN		XB_IN4	UART0_ TX	XB_OUT7	I2C0_SDA	FB_AD8	
A8	113	80	PTC8	HSADC1B _CH11/ CMP0_IN2	HSADC1B _CH11/ CMP0_IN2	PTC8		FTM3_ CH4	eflexPWM 1_A2				FB_AD7	
D7	114	81	PTC9	HSADC1B _CH12/ CMP0_IN3	HSADC1B _CH12/ CMP0_IN3	PTC9		FTM3_ CH5	eflexPWM 1_B2				FB_AD6	
C7	115	82	PTC10	HSADC1B _CH13	HSADC1B _CH13	PTC10	I2C1_SCL	FTM3_ CH6	eflexPWM 1_A3				FB_AD5	
B7	116	83	PTC11/ LLWU_ P11	HSADC1B _CH14	HSADC1B _CH14	PTC11/ LLWU_ P11	I2C1_SDA	FTM3_ CH7	eflexPWM 1_B3				FB_RW_b	
A7	117	84	PTC12	DISABLED		PTC12	CAN2_TX		FTM_ CLKIN0	eflexPWM 1_A1	FTM3_ FLT0	SPI2_ PCS1	FB_AD27	UART4_ RTS_b
D6	118	85	PTC13	DISABLED		PTC13	CAN2_RX		FTM_ CLKIN1	eflexPWM 1_B1			FB_AD26	UART4_ CTS_b
C6	119	86	PTC14	DISABLED		PTC14	I2C1_SCL	I2C0_SCL		eflexPWM 1_A0			FB_AD25	UART4_ RX
B6	120	87	PTC15	DISABLED		PTC15	I2C1_SDA	I2C0_SDA		eflexPWM 1_B0			FB_AD24	UART4_ TX
—	121	88	VSS	VSS	VSS									
—	122	89	VDD	VDD	VDD									
A6	123	90	PTC16	DISABLED		PTC16	CAN1_RX	UART3_ RX	ENET0_ 1588_ TMR0	eflexPWM 1_A2			FB_CS5_ b/ FB_TSIZ1/ FB_BE23_ 16_b	
D5	124	91	PTC17	DISABLED		PTC17	CAN1_TX	UART3_ TX	ENET0_ 1588_ TMR1	eflexPWM 1_B2			FB_CS4_ b/ FB_TSIZ0/ FB_BE31_ 24_b	
C5	125	92	PTC18	DISABLED		PTC18		UART3_ RTS_b	ENET0_ 1588_ TMR2	eflexPWM 1_A3			FB_TBST_ b/ FB_CS2_ b/ FB_BE15_ 8_b	
B5	126	—	PTC19	DISABLED		PTC19		UART3_ CTS_b	ENET0_ 1588_ TMR3	eflexPWM 1_B3			FB_CS3_ b/	FB_TA_b

144 MAP BGA	144 LQFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
													FB_BE7_0_b	
A5	127	93	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FTM0_CH0	eflexPWM0_A0		FB_ALE/ FB_CS1_b/ FB_TS_b	eflexPWM1_A0
D4	128	94	PTD1	HSADC1A_CH11	HSADC1A_CH11	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FTM0_CH1	eflexPWM0_B0		FB_CS0_b	eflexPWM1_B0
C4	129	95	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FTM0_CH2	eflexPWM0_A1	I2C0_SCL	FB_AD4	eflexPWM1_A1
B4	130	96	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FTM0_CH3	eflexPWM0_B1	I2C0_SDA	FB_AD3	eflexPWM1_B1
A4	131	97	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	eflexPWM0_A2	EWM_IN	SPI1_PCS0	FB_AD2	
A3	132	98	PTD5	HSADC1A_CH8	HSADC1A_CH8	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	eflexPWM0_B2	EWM_OUT_b	SPI1_SCK	FB_AD1	
A2	133	99	PTD6/ LLWU_P15	HSADC1A_CH9	HSADC1A_CH9	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI1_SOUT	FB_AD0	
M10	134	—	VSS	VSS	VSS									
F8	135	—	VDD	VDD	VDD									
A1	136	100	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI1_SIN		
C9	137	—	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C1_SCL	UART5_RX			eflexPWM0_A3		FB_A16	
B9	138	—	PTD9	DISABLED		PTD9	I2C1_SDA	UART5_TX			eflexPWM0_B3		FB_A17	
B3	139	—	PTD10	DISABLED		PTD10		UART5_RTS_b			eflexPWM0_A2		FB_A18	
B2	140	—	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25	SPI2_PCS0	UART5_CTS_b			eflexPWM0_B2		FB_A19	
B1	141	—	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	XB_IN5	XB_OUT5	eflexPWM0_A1		FB_A20	
C3	142	—	PTD13	DISABLED		PTD13	SPI2_SOUT		XB_IN7	XB_OUT7	eflexPWM0_B1		FB_A21	
C2	143	—	PTD14	DISABLED		PTD14	SPI2_SIN		XB_IN11	XB_OUT11	eflexPWM0_A0		FB_A22	
C1	144	—	PTD15	DISABLED		PTD15	SPI2_PCS1				eflexPWM0_B0		FB_A23	

5.2 KV5x Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8		PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11/ LLWU_P25	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9		PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8/ LLWU_P24		PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6/ LLWU_P16	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10/ LLWU_P18	PTE9/ LLWU_P17	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	PTE18/ LLWU_P20	PTE19	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	PTE16	PTE17/ LLWU_P19	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	HSADC0A_ CH6	HSADC0A_ CH7/ ADC0_SE4b	ADC0_SE8/ ADC0_DM0/ CMP1_IN2	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	PTE20	PTE21	ADC0_SE0/ ADC0_DP0/ CMP2_IN5	PTE26	PTE25/ LLWU_P21	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	HSADC0A_ CH2/ HSADC1A_ CH2	HSADC0A_ CH3/ HSADC1A_ CH3	PTE30	HSADC0A_ CH12/ CMP0_IN4/ CMP2_IN3	PTE13	VDD	PTA4/ LLWU_P3	PTA9	PTA11/ LLWU_P23	PTA14	PTA15	RESET_b	L
M	HSADC0A_ CH10/ HSADC1B_ CH2	HSADC0A_ CH11/ HSADC1B_ CH3	PTE29	PTE24		PTE23	PTE22	PTA5	PTA10/ LLWU_P22	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 26. 144 MAPBGA Pinout Diagram

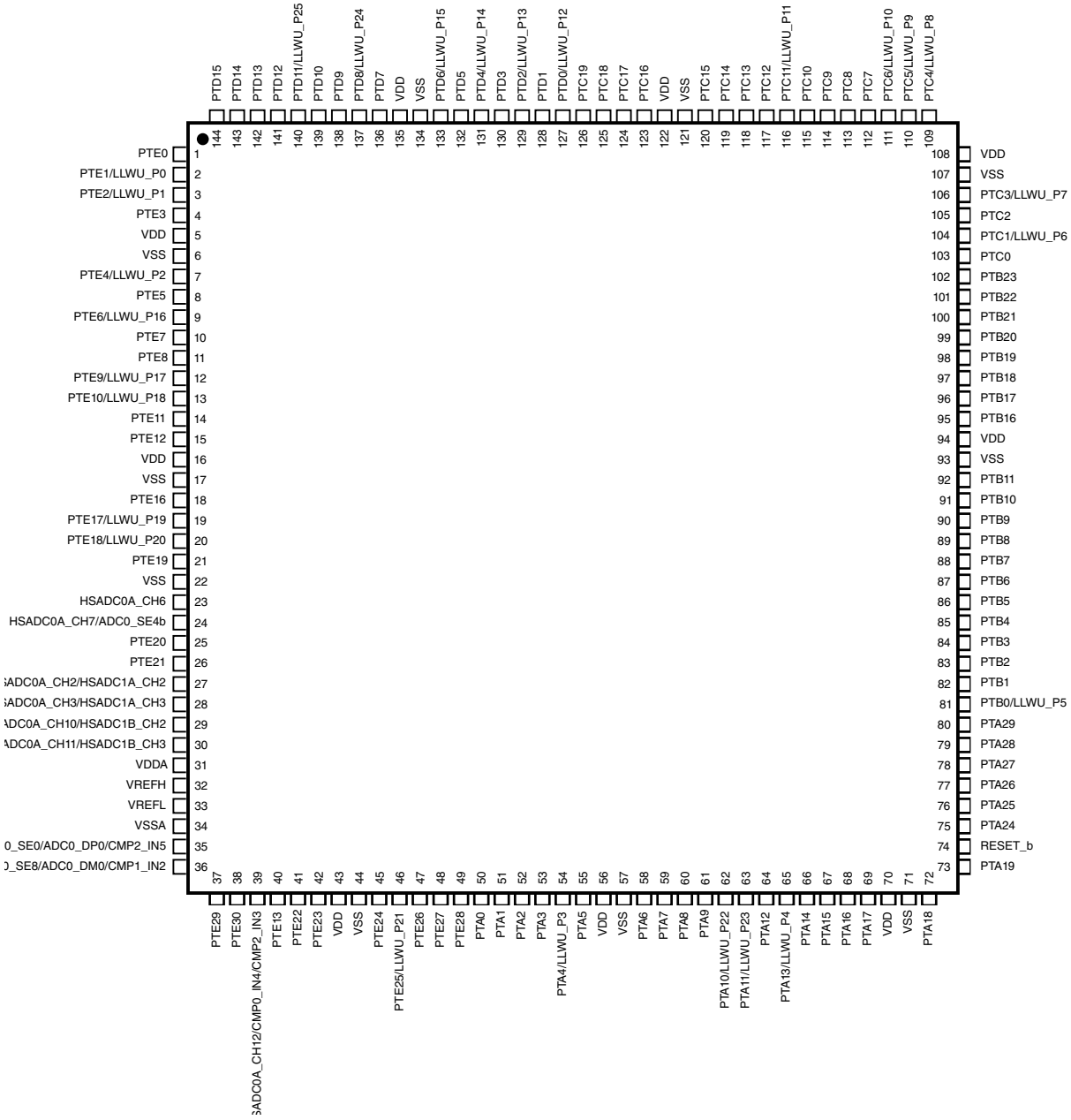


Figure 27. 144 LQFP Pinout Diagram

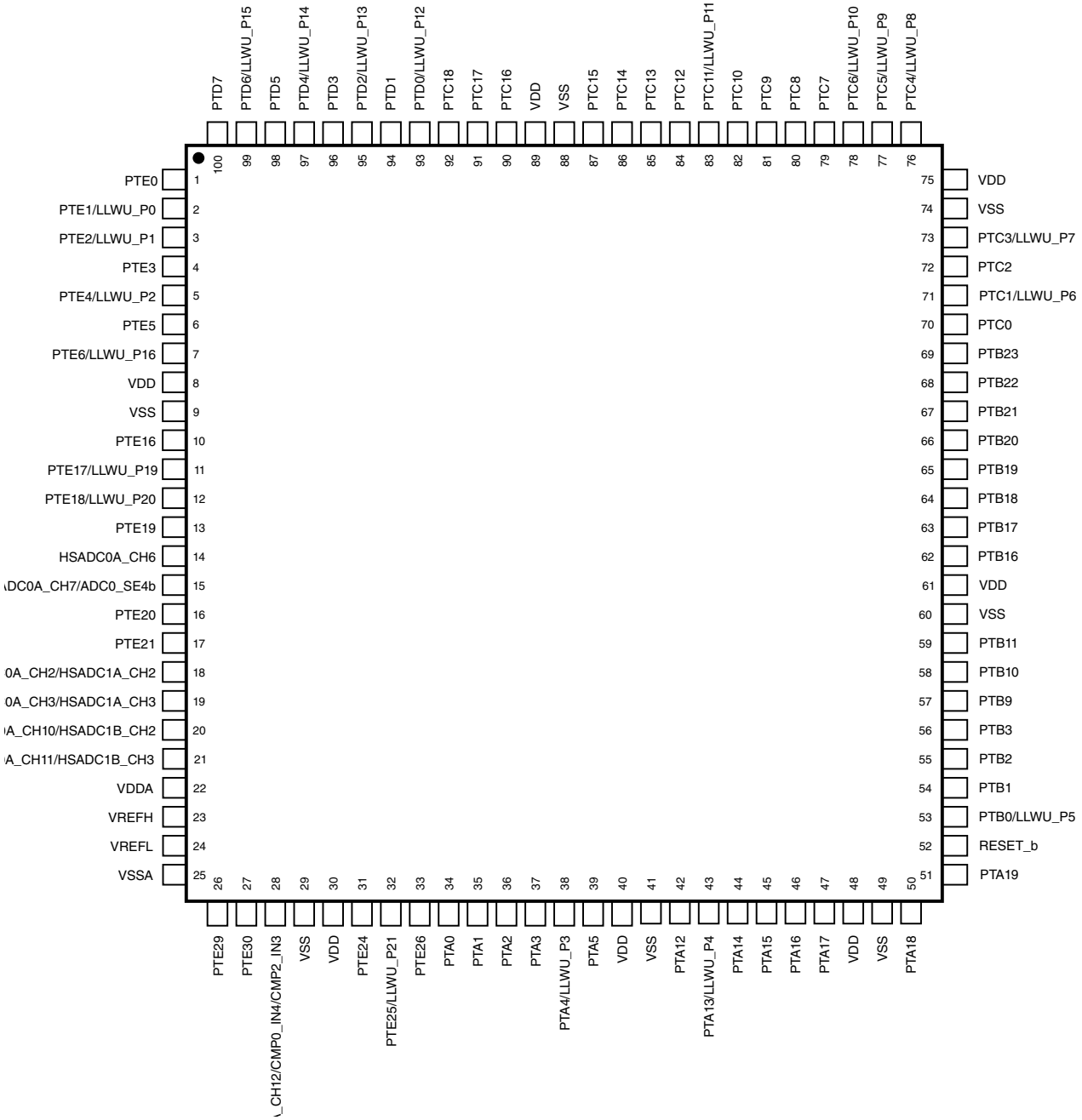


Figure 28. 100 LQFP Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the MKV5x device numbers.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KV## A FFF T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KV##	Kinetis family	• KV58 • KV56
A	Key attribute	• F = Cortex-M7
FFF	Program flash memory size	• 1M0 = 1 MB • 512 = 512 KB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LQ = 144 LQFP (20 mm x 20 mm) • LL = 100 LQFP (14 mm x 14 mm) • MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 24 = 240 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKV58F1M0VLQ24

MKV56F512VLL24

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

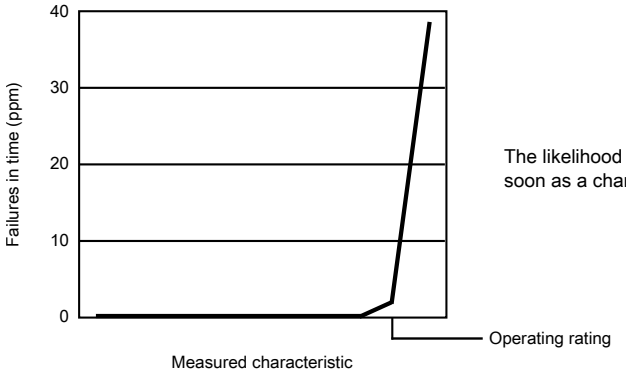
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

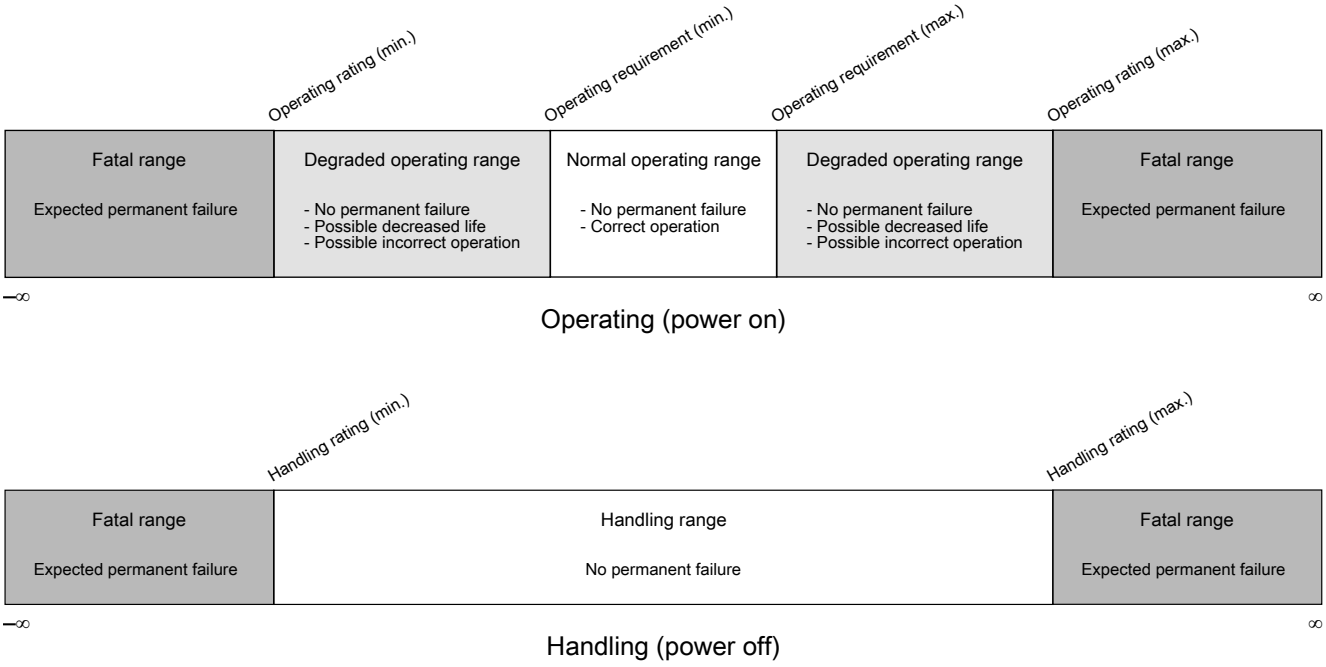
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

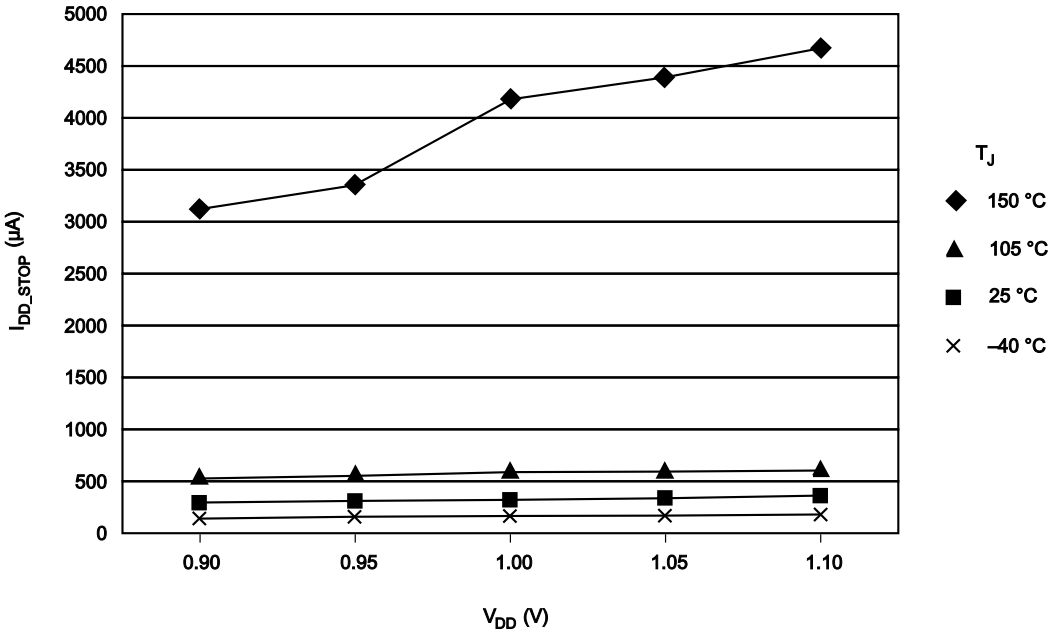
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision History

The following table provides a revision history for this document.

Table 40. Revision History

Rev. No.	Date	Substantial Changes
0	02/2015	Initial release
1	06/2015	• Updated the features list to include FlexBus, TRNG, MMCAU, Advanced WatchDog Timer and JTAG modules • Updated the ordering information table to highlight differences in the parts in terms of flash, SRAM, modules or instances.

Table continues on the next page...

Table 40. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• Added KV5x block diagram
		• Editorial changes in the table "Recommended Operating Conditions."
		• Removed the Typical values column from the table "Recommended Operating Conditions."
		• Removed the following parameters from the table "Recommended Operating Conditions."
		  • Output Source Current High (I_{OH})
		  • Output Source Current Low (I_{OL})
		  • Oscillator Input Voltage High(V_{IHOSC})
		  • Oscillator Input Voltage Low (V_{ILOSC})
		  • DAC Output Current Drive Strength (C_{out})
		• Added HVD characteristics to the table "LVD, and POR operating requirements" and changed the title to HVD, LVD, and POR operating requirements."
		• Added the following parameters to the table "Voltage and current operating behaviors"
		  • Output high current total for all ports (I_{OHT})
		  • Output low current total for all ports (I_{OHL})
		  • Internal pull-down resistance (R_{PD})
		• Removed the footnote "PTC6 and PTC7 are true open drain so have no high drive output transistor so there is no VOH spec for them. These pins must be terminated with a pull-up resistor to VDD" from the table "Voltage and current operating behaviors"
		• Added a note above the table "Low power mode peripheral adders — typical value" suggesting that the values are preliminary data.
		• Updated the notes in the table "Power consumption operating behaviors" for run mode currents with all peripherals disabled.
		• Updated the table "EMC radiated emissions operating behaviors" by splitting description column into Conditions and Clocks columns.
		• Changed Typ. values to TBDs in the table "EMC radiated emissions operating behaviors."
		• Updated the table "Typical device clock specifications"
		• Added a footnote to the ambient temperature entry in the table "Thermal operating requirements"
		• Updated the table "Thermal attributes"
		• Changed ADC to HSADC in the title of the section "12-bit SAR High Speed Analog-to-Digital Converter (ADC) parameters"
		• Changed minimum operating voltage value from 2.7 V to 1.71 V in the table "MII signal switching specifications" and RMII signal switching specifications."

2	10/2015	• Updated the part numbers in the table Orderable part numbers summary and the front page
		• In the features list:
		  • Updated the instances of UART and SPI modules
		  • Added Ether module to the list of communication interfaces
		  • Remove Micro Trace Buffer from the list of System peripherals
		  • In table Operating Requirements, removed rows for N_F, T_R, and t_{FLRET}
		• In table PORT Voltage and current operating behaviors, added I_{ICIO}, I_{ICcont}, and V_{ODPU} rows
		• Updated table Power mode transition operating behaviors
		• Updated table Power consumption operating behaviors
		• Updated table EMC radiated emissions operating behaviors
		• Updated table General switching specifications
		• In section DSPI switching specifications (limited voltage range)
		  • Removed the notes
		  • Removed table "Master mode DSPI timing for fast pads (limited voltage range)"

Table continues on the next page...

Table 40. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed the tbale "Master mode DSPI timing for open drain pads (limited voltage range)" • Removed the table "Slave mode DSPI timing for fast pads (limited voltage range)" • Removed the table "Slave mode DSPI timing for open drain pads (limited voltage range)" • Removed the table "Master mode DSPI timing fast pads (full voltage range)" • Removed the table "Master mode DSPI timing open drain pads (full voltage range)" • Removed the table "Slave mode DSPI timing for fast pads (full voltage range)" • Removed the table "Slave mode DSPI timing for open drain pads (full voltage range)" • Updated the pinouts • Updated table Device clock specifications
3	02/2016	• Added new part numbers for 240 MHz and removed the 220 MHz and 200 MHz part numbers • Updated the document number to reflect change from 220 MHz to 240 MHz • Updated Voltage and current operating ratings • Updated Operating Requirements • Updated VLPS → RUN and STOP → RUN values in Power mode transition operating behaviors • In section Power consumption operating behaviors : • Added a note at the beginning of the table • Updated table to reflect 240 MHz values • Updated Typical device clock specifications • In section MCG specifications, updated the values listed under "PLL"
4	06/2016	• Updated PWM resolution in the introduction to 260 ps • Added table Enhanced NanoEdge PWM characteristics
5	03/2020	• Updated FLEXPWM to eflexPWM all over the document • Updated "Pad leakage due to input protection" to "Pad leakage" in ADC input impedance equivalency diagram in 16-bit ADC operating conditions • Updated the first footnote to "The DAC reference can be selected to be VDDA or VREF_OUT" in 12-bit DAC operating requirements • Updated Voltage and current operating ratings • Updated the title of section and table from "Operating Requirements" to "Voltage and current operating requirements" • Updated the Voltage and current operating ratings table • Updated the section title from "Port Voltage and current operating behaviors" to "Voltage and current operating behaviors" • Removed I_{CIO} and I_{ICcont} from Voltage and current operating behaviors table • Updated title from "Typical device clock specifications" to "Device clock specifications" • Updated the description in General switching specifications table • Added HSADC Input Resolution Table in 12-bit SAR High Speed Analog-to-Digital Converter (HSADC) parameters

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