





SN54AHCT86, SN74AHCT86 SCLS250P - OCTOBER 1995 - REVISED OCTOBER 2023

145

SNx4AHCT86 Quadruple 2-Input Exclusive-OR Gates

1 Features

Texas

INSTRUMENTS

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.
- ESD protection exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

2 Applications

- Server
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- **Telecom infrastructures**
- Electronic points-of-sale

3 Description

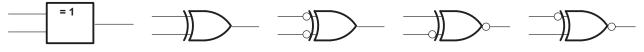
The SNx4AHCT86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \times B$ or $Y = \overline{AB} + A \overline{B}$ in positive logic.

Package Information ⁽¹⁾										
PART NUMBER	PACKAGE	BODY SIZE (NOM)								
	J (CDIP, 14)	19.56 mm × 6.67 mm								
SN54AHCT86	W (CFP, 14)	13.09 mm × 6.92 mm								
	FK (LCCC, 20)	8.89 mm × 8.89 mm								
	N (PDIP , 14)	19.3 mm × 6.35 mm								
	D (SOIC, 14)	8.65 mm × 3.91 mm								
	NS (SOP, 14)	10.30 mm × 5.30 mm								
SN74AHCT86	DB (SSOP, 14)	6.20 mm × 5.30 mm								
SN/4ARC100	PW (TSSOP, 14)	5.00 mm × 4.40 mm								
	DGV (TVSOP, 14)	3.60 mm × 4.40 mm								
	RGY (VQFN, 14)	3.50 mm × 3.50 mm								
	BQA (WQFN, 14)	3.00 mm × 2.50 mm								

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR



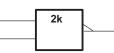
These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



The output is active (low) if all inputs stand at the same logic level (that is, A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (that is, 0 or 2) are active.

Simplified Schematic

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (that is, only 1 of the 2) are active.





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

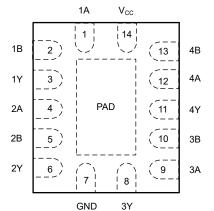
С	Changes from Revision O (May 2023) to Revision P (October 2023)	Page
•	Updated R θ JA values: D = 97.5 to 124.5, PW = 125.1 to 147.7; Updated D and PW packages for R θ R θ JB, Ψ JT, Ψ JB, and R θ JC(bot), all values in °C/W	
С	Changes from Revision N (August 2014) to Revision O (May 2023)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Updated Package Information table	1
		· · · · · · · · · · · · · · · · · · ·



5 Pin Configuration and Functions

1A 🖂 10 14 🗔 V_{cc} 13 🗖 4B 1B 🗖 2 1Y 🖂 12 🗖 4A 3 2A 🖂 11 🗖 4Y 4 2B 🗖 10 🗔 3B 5 ____ ЗА 2Y 🖂 6 9 GND 🗔 7 8 ____ 3Y

Figure 5-1. SN54AHCT86 J or W Package, 14-Pin (Top View) SN74AHCT86 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)





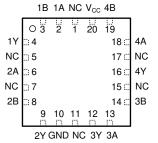


Figure 5-3. SN54AHCT86 FK Package, 20-Pin (Top View)

		PIN				
	SN74A	HCT86	SN54A	HCT86	TYPE ⁽¹⁾	DESCRIPTION
NAME	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
1A	1	1	1	2	I	1A Input
1B	2	2	2	3	I	1B Input
1Y	3	3	3	4	0	1Y Output
2A	4	4	4	6	I	2A Input
2B	5	5	5	8	I	2B Input
2Y	6	6	6	9	0	2Y Output
3Y	8	8	8	12	0	3Y Output
3A	9	9	9	13	I	3A Input
3B	10	10	10	14	I	3B Input
4Y	11	11	11	16	0	4Y Output
4A	12	12	12	18	I	4A Input
4B	13	13	13	19	I	4B Input
GND	7	7	7	10	_	Ground Pin
NC	_	_	_	1, 5, 7, 11, 15, 17	_	No Connection
V _{CC}	14	14	14	20	_	Power Pin

Table 5-1. Pin Functions



Table 5-1. Pin Functions (continued)

		PIN					
	SN74A	HCT86	SN54A	HCT86	TYPE ⁽¹⁾	DESCRIPTION	
NAME	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK			
Thermal Pad	_	PAD	_	_	_	Thermal Pad	

(1) I = input, O = output



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	$V_{O} < 0 \text{ or } V_{O} > V_{CC}$		±20	mA
I _O	Continuous output current	$V_{O} = 0$ to V_{CC}		±25	mA
	Continuous current through $V_{\mbox{\scriptsize CC}}$ or GND			±50	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT			
T _{stg}	Storage temperature rang	ige temperature range						
V	Electrostatic discharge	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾		2000	V			
V _(ESD)	Electrostatic discharge			1000	v			

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AH	СТ86	SN74AH0	СТ86	UNIT
		MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	125	°C

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

6.4 Thermal Information

		SNx4AHCT86								
	THERMAL METRIC ⁽¹⁾	D	DB	DGV	N	NS	PW	RGY	BQA	UNIT
					14 PI	NS				
R _{θJA}	Junction-to-ambient thermal resistance	124.5	109.5	133.3	59.7	92.2	147.7	59.0	88.3	
R _{0JC(top)}	Junction-to-case (top) thermal resistance	78.8	62.1	55.6	47.3	49.8	77.4	72.5	90.9	
R _{θJB}	Junction-to-board thermal resistance	81	56.9	66.3	39.5	51.0	90.9	35.0	56.8	
Ψյт	Junction-to-top characterization parameter	37	22.6	7.8	32.4	15.7	27.2	3.9	9.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	80.6	56.3	56.6	39.4	50.6	90.2	35.1	56.7	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	15.4	33.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	т	T _A = 25°C S		SN54AHCT86		–40°C to 85°C SN74AHCT86		–40°C to 125°C SN74AHCT86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I _{OH} = −8 mA	4.5 V	3.94			3.8		3.8		3.8		v
V	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1		0.1	V
V _{OL}	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44		0.44	v
I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		±1	μA
Icc	$V_{I} = V_{CC}$ or GND, $I_{O} = 0$	5.5 V			2		20		20		20	μA
ΔI_{CC} ⁽²⁾	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
Ci	V _I = V _{CC} or GND	5 V		4	10				10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

		0						•			/ \	•	,
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE			T _A = 25°C		–55°C to 125°C SN54AHCT86		-40°C to 85°C SN74AHCT86		-40°C to 125°C SN74AHCT86	
	(INPOT)	(001P01)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	v	C ₁ = 15 pF		5 <mark>(1)</mark>	6.9 <mark>(1)</mark>	1(1)	8 ⁽¹⁾	1	8	1	9	ns
t _{PHL}	AOIB	T	CL = 15 pF		5 <mark>(1)</mark>	6.9 <mark>(1)</mark>	1(1)	8 ⁽¹⁾	1	8	1	9	115
t _{PLH}	A or B	v	C ₁ = 50 pF		5.5	8.8	1	10	1	9	1	11	ns
t _{PHL}	AUD		0L = 30 pi		5.5	8.8	1	10	1	9	1	11	115

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



6.7 Noise Characteristics

 $V_{CC} = 5 V, C_L = 50 pF, T_A = 25^{\circ}C^{(1)}$

	PARAMETER	SN	UNIT		
	FARAIMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.4	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.4	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4			V
V _{IH(D)}	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

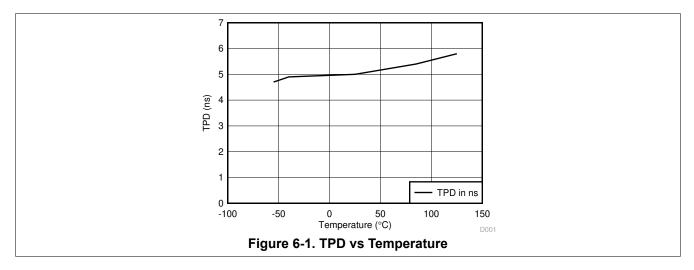
(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

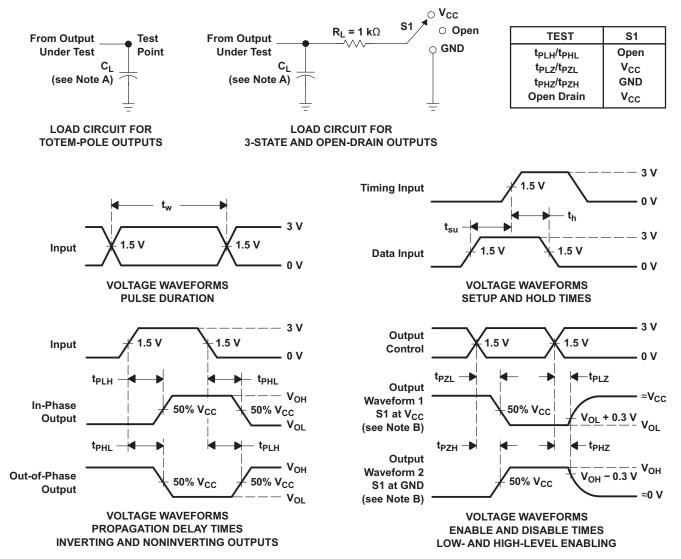
	PARAMETER	TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

6.9 Typical Characteristics





7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r \leq 3 ns, t_f \leq 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms



8 Detailed Description

8.1 Overview

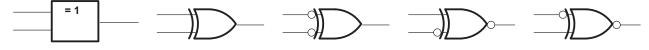
The SNx4AHCT86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \times B$ or $Y = \overline{AB} + A \overline{B}$ in positive logic.

The inputs are TTL compatible allowing 3.3 V to 5 V translation.

8.2 Functional Block Diagram

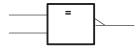
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR



These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



The output is active (low) if all inputs stand at the same logic level (that is, A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (that is, 0 or 2) are active.

Figure 8-1. Exclusive-OR Logic

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (that is, only 1 of the 2) are active.

8.3 Feature Description

- TTL inputs
 - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

8.4 Device Functional Modes

	(Each Gate)								
INP	UTS	OUTPUT							
Α	В	Y							
L	L	L							
L	Н	н							
н	L	н							
н	Н	L							

Table 8-1. Function Table



9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4AHCT86 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes the device ideal for translating up from 3.3 V to 5 V. Figure 9-2 shows this type of translation.

9.2 Typical Application

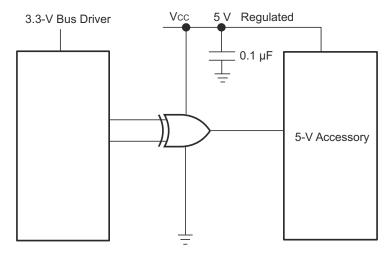


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

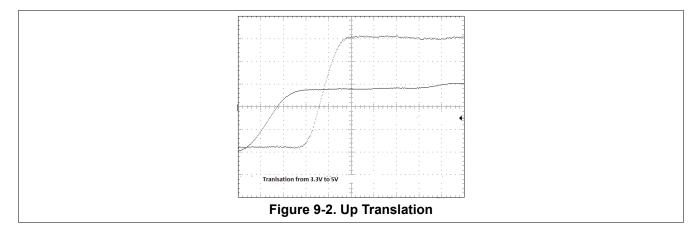
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended input conditions:
 - Rise time and fall time specs: see (Δt/ΔV) in the *Recommended Operating Conditions* table.
 - Specified High and low levels: see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- 2. Recommend output conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part
 - Outputs should not be pulled above $V_{\mbox{\scriptsize CC}}$



9.2.3 Application Curves



9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

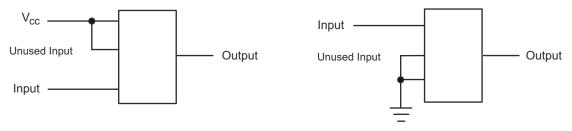
9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 9-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they cannot float when disabled.

9.4.2 Layout Example







10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9681701Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK
5962-9681701QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J
SN74AHCT86BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AHCT86
SN74AHCT86DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT86N
SN74AHCT86N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT86N
SN74AHCT86NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86PW	Obsolete	Production	TSSOP (PW) 14		-	Call TI	Call TI	-40 to 125	HB86
SN74AHCT86PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SN74AHCT86RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SN74AHCT86RGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SNJ54AHCT86FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK



Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT86FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK
SNJ54AHCT86J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J
SNJ54AHCT86J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AHCT86, SN74AHCT86 :

• Catalog : SN74AHCT86

• Military : SN54AHCT86

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications

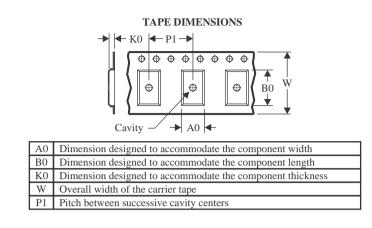


Texas

STRUMENTS

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT86DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT86NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHCT86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT86RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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PACKAGE MATERIALS INFORMATION

23-Jul-2025



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT86DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHCT86DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHCT86DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHCT86NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHCT86PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT86RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

TEXAS INSTRUMENTS

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23-Jul-2025

TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
5962-9681701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74AHCT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT86FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not

- exceed 0.15 mm per side. 4. Reference JEDEC registration MO-150.



DB0014A

EXAMPLE BOARD LAYOUT

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DB0014A

EXAMPLE STENCIL DESIGN

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.



FK 20

8.89 x 8.89, 1.27 mm pitch

GENERIC PACKAGE VIEW

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



J0014A

EXAMPLE BOARD LAYOUT

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE





N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0014A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0014A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



RGY 14

3.5 x 3.5, 0.5 mm pitch

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

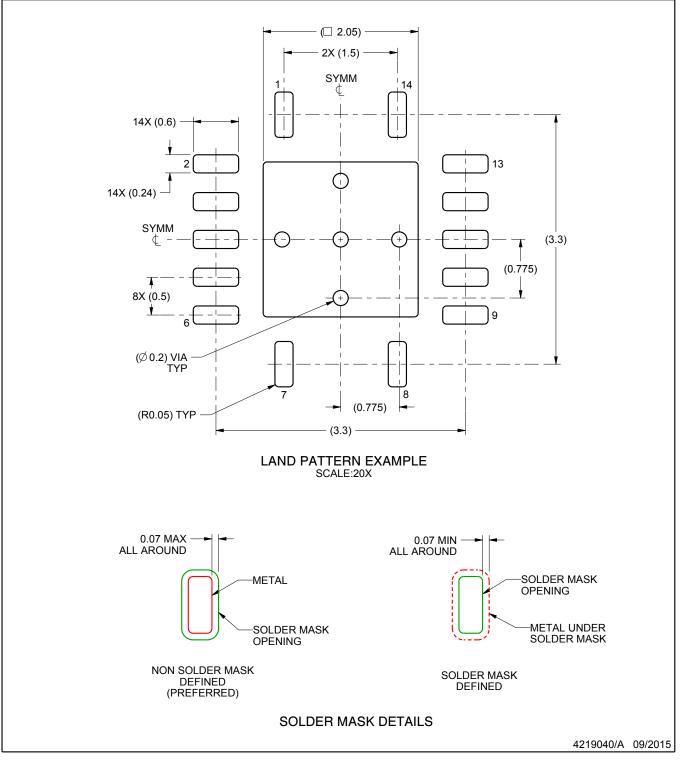


RGY0014A

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



RGY0014A

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



D0014A

EXAMPLE BOARD LAYOUT

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



D0014A

EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



BQA 14

2.5 x 3, 0.5 mm pitch

GENERIC PACKAGE VIEW

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





BQA0014A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



BQA0014A

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



BQA0014A

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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