

### FEATURES

- Low  $V_{os}$ : 75  $\mu\text{V}$  maximum
- Low  $V_{os}$  drift: 1.3  $\mu\text{V}/^\circ\text{C}$  maximum
- Ultrastable vs. time: 1.5  $\mu\text{V}$  per month maximum
- Low noise: 0.6  $\mu\text{V}$  p-p maximum
- Wide input voltage range:  $\pm 14\text{ V}$  typical
- Wide supply voltage range:  $\pm 3\text{ V}$  to  $\pm 18\text{ V}$
- 125 $^\circ\text{C}$  temperature-tested dice

### APPLICATIONS

- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls
  - Thermocouples
  - Resistor thermal detectors (RTDs)
  - Strain bridges
  - Shunt current measurements
- Precision filters

### GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75  $\mu\text{V}$  maximum for OP07E) that is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current ( $\pm 4\text{ nA}$  for the OP07E) and high open-loop gain (200 V/mV for the OP07E). The low offset and high open-loop gain make the OP07 particularly useful for high gain instrumentation applications.

### PIN CONFIGURATION

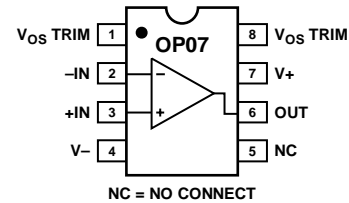
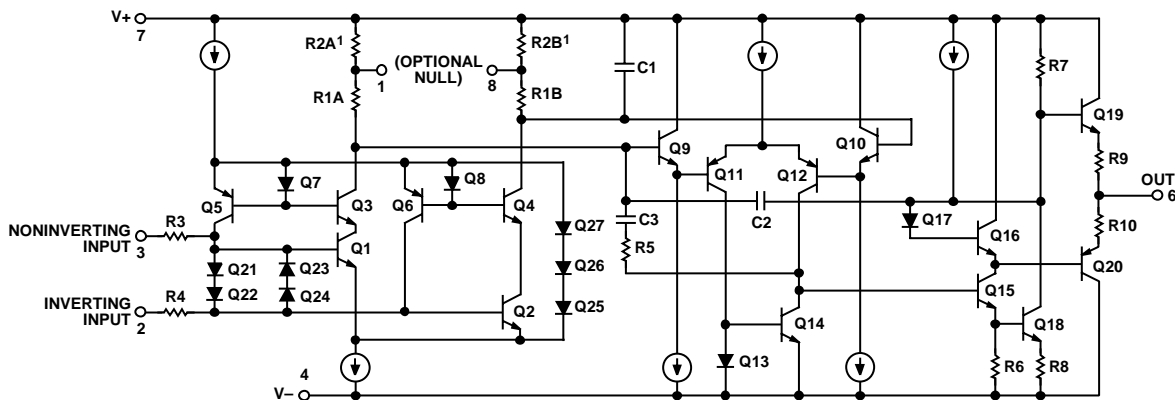


Figure 1.

The wide input voltage range of  $\pm 13\text{ V}$  minimum combined with a high CMRR of 106 dB (OP07E) and high input impedance provide high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications.

The OP07 is available in two standard performance grades. The OP07E is specified for operation over the  $0^\circ\text{C}$  to  $70^\circ\text{C}$  range, and the OP07C is specified over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.

The OP07 is available in epoxy 8-lead PDIP and 8-lead narrow SOIC packages. For CERDIP and TO-99 packages and standard microcircuit drawing (SMD) versions, see the OP77.



<sup>1</sup> R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

Figure 2. Simplified Schematic

### Rev. G

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**REVISION HISTORY**

**10/11—Rev. F. to Rev G**

Changes to Features Section..... 1

**8/10—Rev. E. to Rev F**

Changes to Ordering Guide ..... 14

**7/09—Rev. D. to Rev E**

Changes to Figure 29 Caption..... 11

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**7/06—Rev. C. to Rev D**

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**8/03—Rev. B to Rev. C**

Changes to OP07E Electrical Specifications.....2

Changes to OP07C Electrical Specifications .....3

Edits to Ordering Guide .....5

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Updated Outline Dimensions ..... 11

**3/03—Rev. A to Rev. B**

Updated Package Titles..... Universal

Updated Outline Dimensions ..... 11

**2/02—Rev. 0 to Rev. A**

Edits to Features.....1

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## SPECIFICATIONS

## OP07E ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
<b><math>T_A = 25^\circ\text{C}</math></b>						
Input Offset Voltage <sup>1</sup>	$V_{OS}$			30	75	$\mu\text{V}$
Long-Term $V_{OS}$ Stability <sup>2</sup>	$V_{OS}/\text{Time}$			0.3	1.5	$\mu\text{V}/\text{Month}$
Input Offset Current	$I_{OS}$			0.5	3.8	nA
Input Bias Current	$I_B$			$\pm 1.2$	$\pm 4.0$	nA
Input Noise Voltage	$e_n$ p-p	0.1 Hz to 10 Hz <sup>3</sup>		0.35	0.6	$\mu\text{V}$ p-p
Input Noise Voltage Density	$e_n$	$f_0 = 10\text{ Hz}$		10.3	18.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}^3$		10.0	13.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		9.6	11.0	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current	$I_n$ p-p			14	30	$\text{pA}$ p-p
Input Noise Current Density	$I_n$	$f_0 = 10\text{ Hz}$		0.32	0.80	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}^3$		0.14	0.23	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		0.12	0.17	$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance, Differential Mode <sup>4</sup>	$R_{IN}$		15	50		$\text{M}\Omega$
Input Resistance, Common Mode	$R_{INCM}$			160		$\text{G}\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	106	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		5	20	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	200	500		$\text{V}/\text{mV}$
		$R_L \geq 500\ \Omega, V_O = \pm 0.5\text{ V}, V_S = \pm 3\text{ V}^4$	150	400		$\text{V}/\text{mV}$
<b><math>0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}</math></b>						
Input Offset Voltage <sup>1</sup>	$V_{OS}$			45	130	$\mu\text{V}$
Voltage Drift Without External Trim <sup>4</sup>	$TCV_{OS}$			0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Voltage Drift with External Trim <sup>3</sup>	$TCV_{OSN}$	$R_P = 20\text{ k}\Omega$		0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$			0.9	5.3	nA
Input Offset Current Drift	$TCI_{OS}$			8	35	$\text{pA}/^\circ\text{C}$
Input Bias Current	$I_B$			$\pm 1.5$	$\pm 5.5$	nA
Input Bias Current Drift	$TCI_B$			13	35	$\text{pA}/^\circ\text{C}$
Input Voltage Range	IVR		$\pm 13$	$\pm 13.5$		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	103	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		7	32	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	180	450		$\text{V}/\text{mV}$
<b>OUTPUT CHARACTERISTICS</b>						
<b><math>T_A = 25^\circ\text{C}</math></b>						
Output Voltage Swing	$V_O$	$R_L \geq 10\text{ k}\Omega$	$\pm 12.5$	$\pm 13.0$		V
		$R_L \geq 2\text{ k}\Omega$	$\pm 12.0$	$\pm 12.8$		V
		$R_L \geq 1\text{ k}\Omega$	$\pm 10.5$	$\pm 12.0$		V
<b><math>0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}</math></b>						
Output Voltage Swing	$V_O$	$R_L \geq 2\text{ k}\Omega$	$\pm 12$	$\pm 12.6$		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>						
<b>T<sub>A</sub> = 25°C</b>						
Slew Rate	SR	R <sub>L</sub> ≥ 2 kΩ <sup>3</sup>	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A <sub>VOL</sub> = 1 <sup>5</sup>	0.4	0.6		MHz
Open-Loop Output Resistance	R <sub>O</sub>	V <sub>O</sub> = 0, I <sub>O</sub> = 0		60		Ω
Power Consumption	P <sub>d</sub>	V <sub>S</sub> = ±15 V, No load		75	120	mW
		V <sub>S</sub> = ±3 V, No load		4	6	mW
Offset Adjustment Range		R <sub>P</sub> = 20 kΩ		±4		mV

<sup>1</sup> Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

<sup>2</sup> Long-term input offset voltage stability refers to the averaged trend time of V<sub>OS</sub> vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V<sub>OS</sub> during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.

<sup>3</sup> Sample tested.

<sup>4</sup> Guaranteed by design.

<sup>5</sup> Guaranteed but not tested.

## OP07C ELECTRICAL CHARACTERISTICS

V<sub>S</sub> = ±15 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
<b>T<sub>A</sub> = 25°C</b>						
Input Offset Voltage <sup>1</sup>	V <sub>OS</sub>			60	150	μV
Long-Term V <sub>OS</sub> Stability <sup>2</sup>	V <sub>OS</sub> /Time			0.4	2.0	μV/Month
Input Offset Current	I <sub>OS</sub>			0.8	6.0	nA
Input Bias Current	I <sub>B</sub>			±1.8	±7.0	nA
Input Noise Voltage	e <sub>n</sub> p-p	0.1 Hz to 10 Hz <sup>3</sup>		0.38	0.65	μV p-p
Input Noise Voltage Density	e <sub>n</sub>	f <sub>O</sub> = 10 Hz		10.5	20.0	nV/√Hz
		f <sub>O</sub> = 100 Hz <sup>3</sup>		10.2	13.5	nV/√Hz
		f <sub>O</sub> = 1 kHz		9.8	11.5	nV/√Hz
Input Noise Current	I <sub>n</sub> p-p			15	35	pA p-p
Input Noise Current Density	I <sub>n</sub>	f <sub>O</sub> = 10 Hz		0.35	0.90	pA/√Hz
		f <sub>O</sub> = 100 Hz <sup>3</sup>		0.15	0.27	pA/√Hz
		f <sub>O</sub> = 1 kHz		0.13	0.18	pA/√Hz
Input Resistance, Differential Mode <sup>4</sup>	R <sub>IN</sub>		8	33		MΩ
Input Resistance, Common Mode	R <sub>INCM</sub>			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = ±13 V	100	120		dB
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = ±3 V to ±18 V		7	32	μV/V
Large Signal Voltage Gain	A <sub>VO</sub>	R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V	120	400		V/mV
		R <sub>L</sub> ≥ 500 Ω, V <sub>O</sub> = ±0.5 V, V <sub>S</sub> = ±3 V <sup>4</sup>	100	400		V/mV
<b>-40°C ≤ T<sub>A</sub> ≤ +85°C</b>						
Input Offset Voltage <sup>1</sup>	V <sub>OS</sub>			85	250	μV
Voltage Drift Without External Trim <sup>4</sup>	TCV <sub>OS</sub>			0.5	1.8	μV/°C
Voltage Drift with External Trim <sup>3</sup>	TCV <sub>OSN</sub>	R <sub>P</sub> = 20 kΩ		0.4	1.6	μV/°C
Input Offset Current	I <sub>OS</sub>			1.6	8.0	nA
Input Offset Current Drift	TCI <sub>OS</sub>			12	50	pA/°C
Input Bias Current	I <sub>B</sub>			±2.2	±9.0	nA
Input Bias Current Drift	TCI <sub>B</sub>			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = ±13 V	97	120		dB
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = ±3 V to ±18 V		10	51	μV/V
Large Signal Voltage Gain	A <sub>VO</sub>	R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V	100	400		V/mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>OUTPUT CHARACTERISTICS</b>						
<b>T<sub>A</sub> = 25°C</b>						
Output Voltage Swing	V <sub>O</sub>	R <sub>L</sub> ≥ 10 kΩ	±12.0	±13.0		V
		R <sub>L</sub> ≥ 2 kΩ	±11.5	±12.8		V
		R <sub>L</sub> ≥ 1 kΩ		±12.0		V
<b>-40°C ≤ T<sub>A</sub> ≤ +85°C</b>						
Output Voltage Swing	V <sub>O</sub>	R <sub>L</sub> ≥ 2 kΩ	±12	±12.6		V
<b>DYNAMIC PERFORMANCE</b>						
<b>T<sub>A</sub> = 25°C</b>						
Slew Rate	SR	R <sub>L</sub> ≥ 2 kΩ <sup>3</sup>	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A <sub>VOL</sub> = 1 <sup>5</sup>	0.4	0.6		MHz
Open-Loop Output Resistance	R <sub>O</sub>	V <sub>O</sub> = 0, I <sub>O</sub> = 0		60		Ω
Power Consumption	P <sub>d</sub>	V <sub>S</sub> = ±15 V, No load		80	150	mW
		V <sub>S</sub> = ±3 V, No load		4	8	mW
Offset Adjustment Range		R <sub>P</sub> = 20 kΩ		±4		mV

<sup>1</sup> Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

<sup>2</sup> Long-term input offset voltage stability refers to the averaged trend time of V<sub>OS</sub> vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V<sub>OS</sub> during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.

<sup>3</sup> Sample tested.

<sup>4</sup> Guaranteed by design.

<sup>5</sup> Guaranteed but not tested.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage (V <sub>s</sub> )	±22 V
Input Voltage <sup>1</sup>	±22 V
Differential Input Voltage	±30 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range S and P Packages	–65°C to +125°C
Operating Temperature Range OP07E	0°C to 70°C
OP07C	–40°C to +85°C
Junction Temperature	150°C
Lead Temperature, Soldering (60 sec)	300°C

<sup>1</sup>For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC_N (S-Suffix)	158	43	°C/W

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# TYPICAL PERFORMANCE CHARACTERISTICS

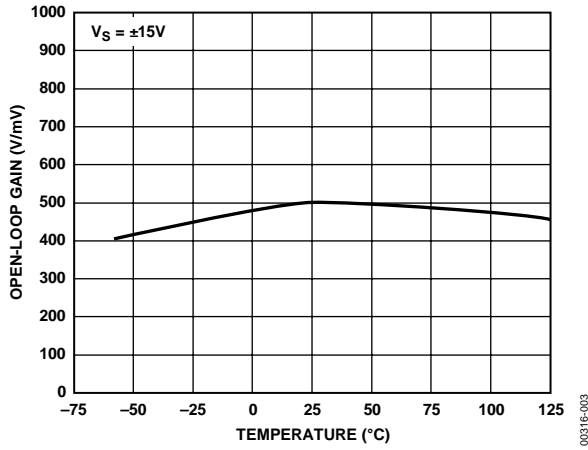


Figure 3. Open-Loop Gain vs. Temperature

00316-003

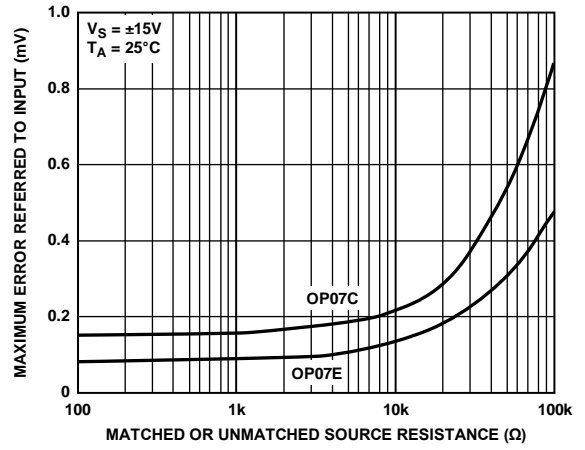


Figure 6. Maximum Error vs. Source Resistance

00316-006

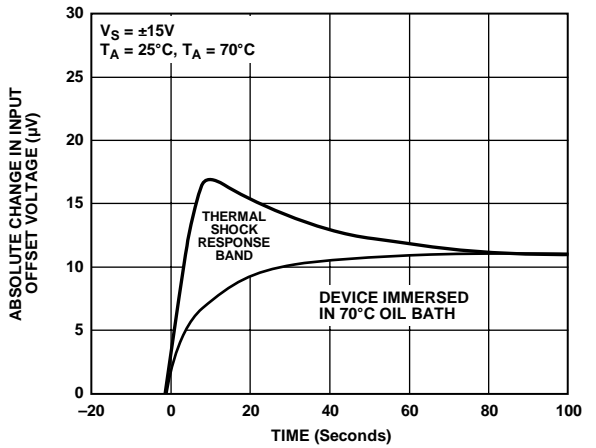


Figure 4. Offset Voltage Change due to Thermal Shock

00316-004

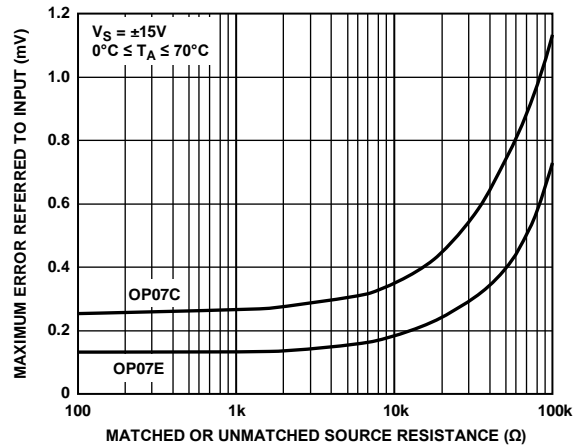


Figure 7. Maximum Error vs. Source Resistance

00316-007

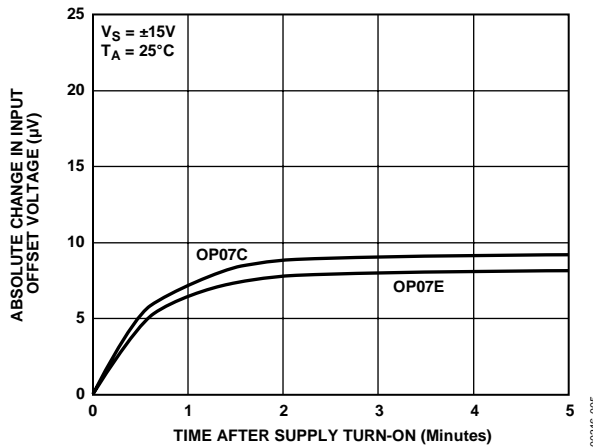


Figure 5. Warm-Up Drift

00316-005

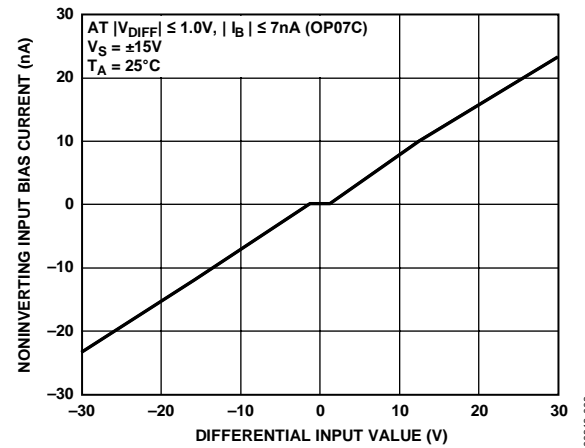


Figure 8. Input Bias Current vs. Differential Input Voltage

00316-008

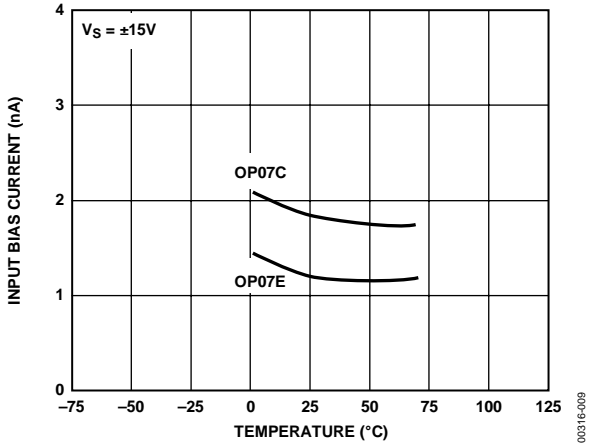


Figure 9. Input Bias Current vs. Temperature

00316-009

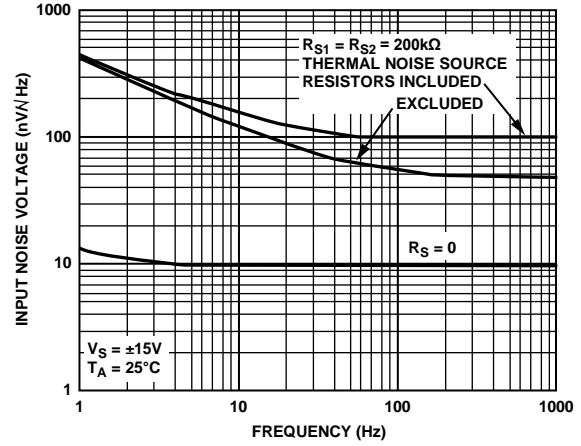


Figure 12. Total Input Noise Voltage vs. Frequency

00316-012

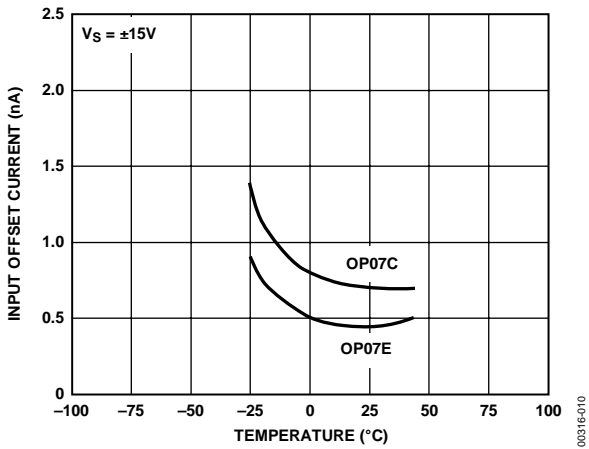


Figure 10. Input Offset Current vs. Temperature

00316-010

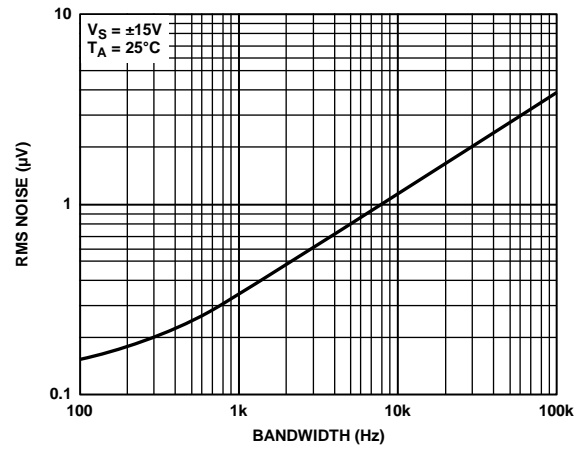


Figure 13. Input Wideband Noise vs. Bandwidth, 0.1 Hz to Frequency Indicated

00316-013

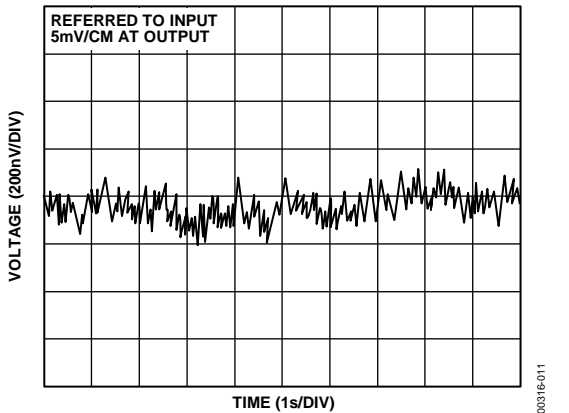


Figure 11. Low Frequency Noise

00316-011

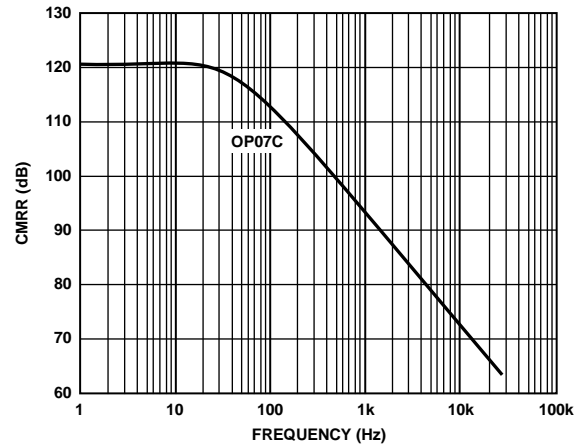


Figure 14. CMRR vs. Frequency

00316-014



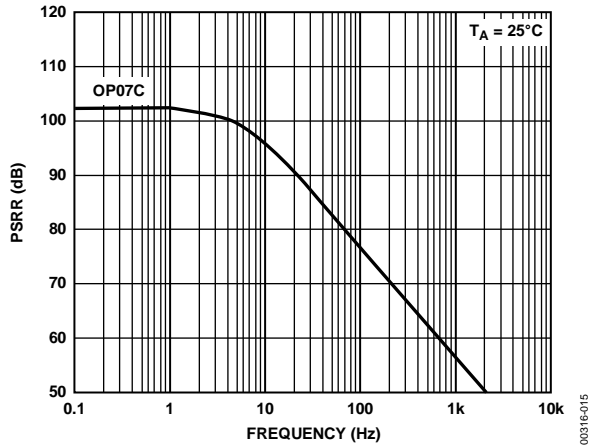


Figure 15. PSRR vs. Frequency

00316-015

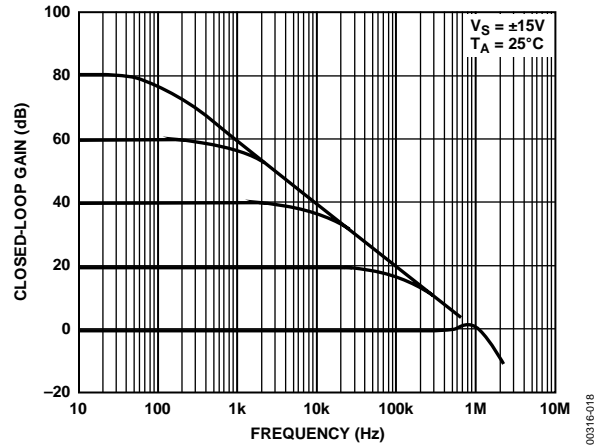


Figure 18. Closed-Loop Frequency Response for Various Gain Configurations

00316-018

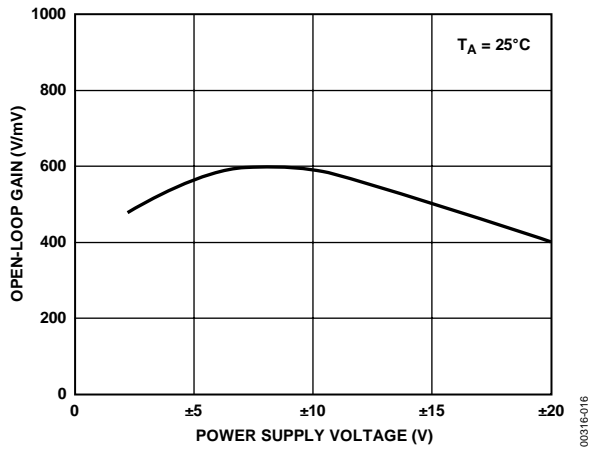


Figure 16. Open-Loop Gain vs. Power Supply Voltage

00316-016

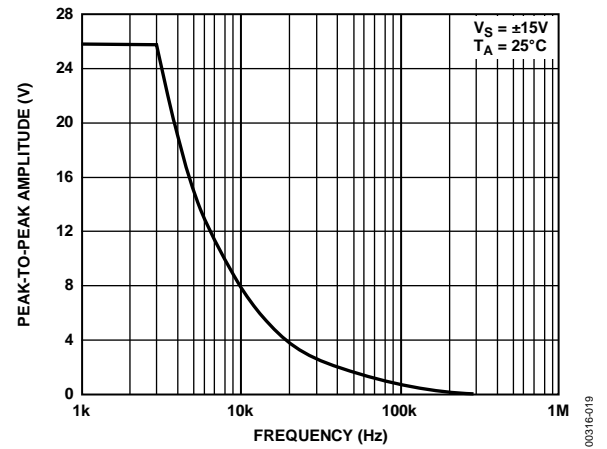


Figure 19. Maximum Output Swing vs. Frequency

00316-019

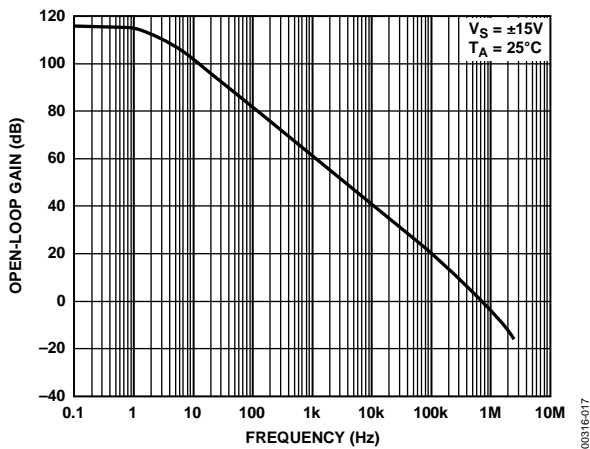


Figure 17. Open-Loop Frequency Response

00316-017

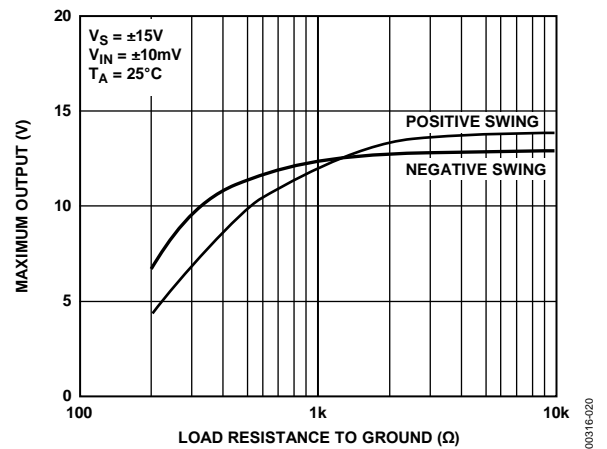


Figure 20. Maximum Output Voltage vs. Load Resistance

00316-020

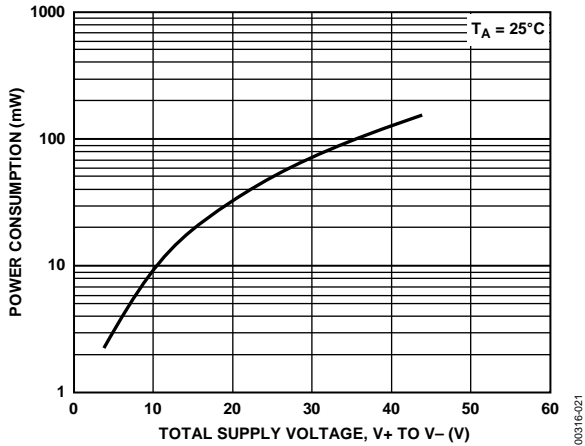


Figure 21. Power Consumption vs. Power Supply

00316-021

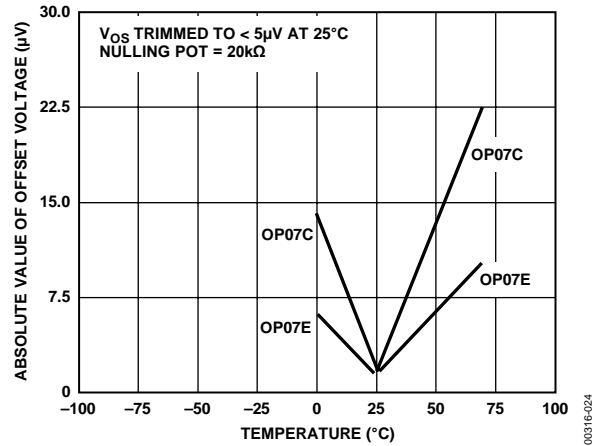


Figure 24. Trimmed Offset Voltage vs. Temperature

00316-024

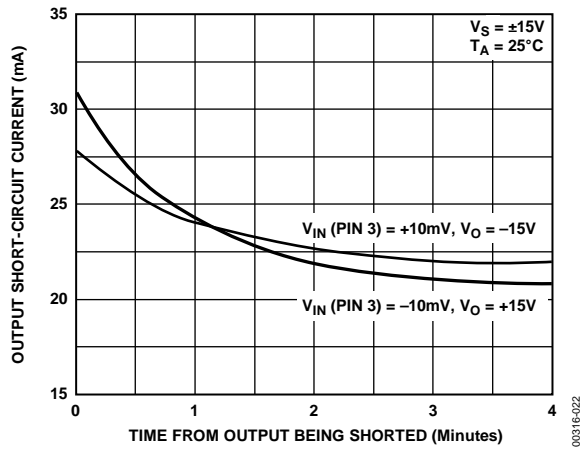


Figure 22. Output Short-Circuit Current vs. Time

00316-022

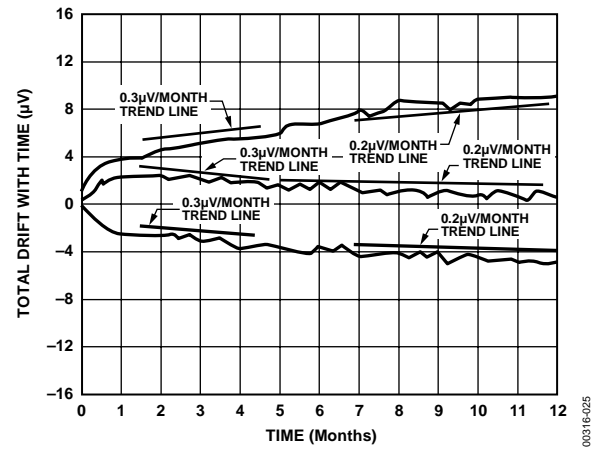


Figure 25. Offset Voltage Drift vs. Time

00316-025

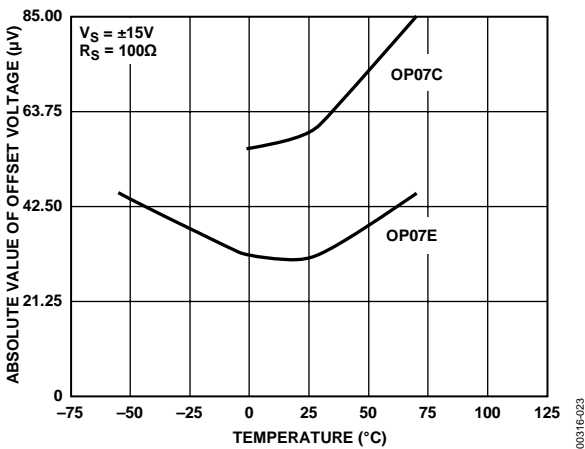


Figure 23. Untrimmed Offset Voltage vs. Temperature

00316-023

TYPICAL APPLICATIONS

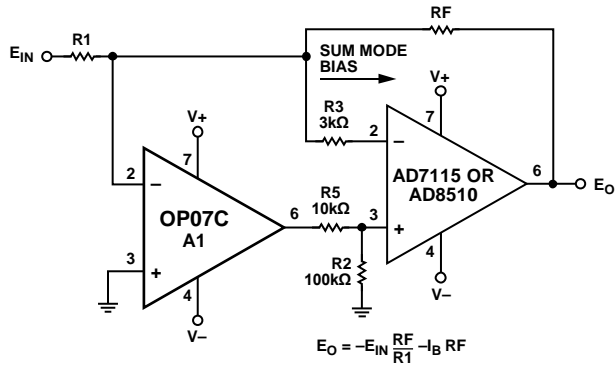


Figure 26. Typical Offset Voltage Test Circuit

00316-026

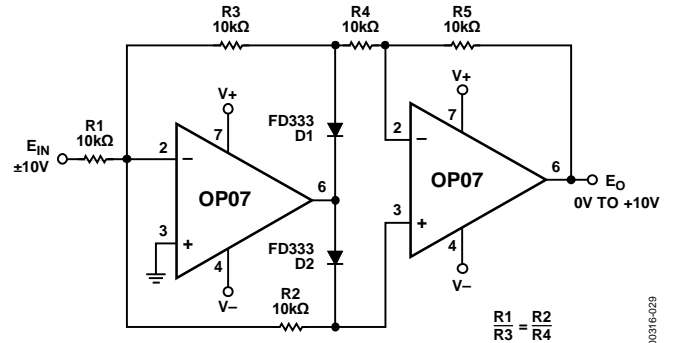


Figure 29. Absolute Value Circuit

00316-029

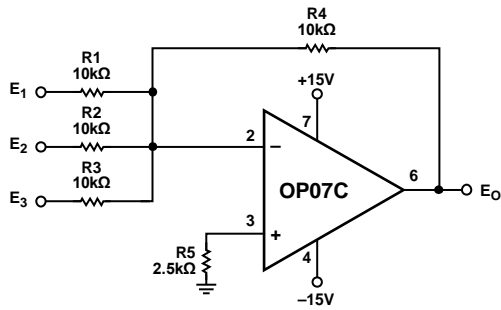
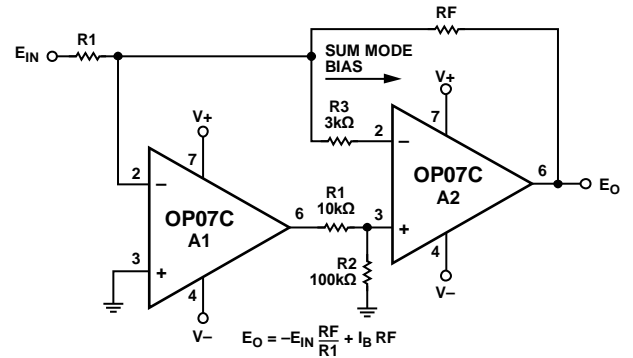


Figure 27. Typical Low Frequency Noise Circuit

00316-027



NOTES  
1. PINOUT SHOWN FOR P PACKAGE

Figure 30. High Speed, Low Vos Composite Amplifier

00316-030

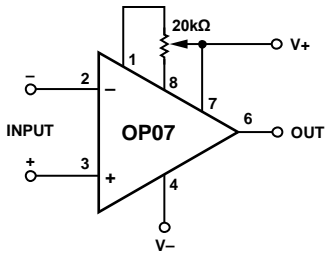
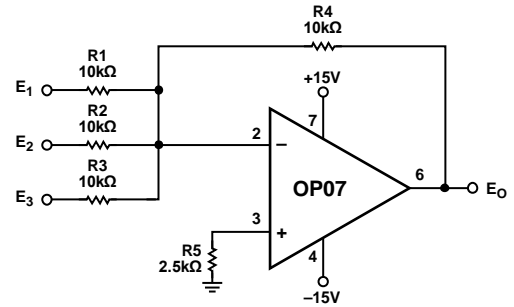


Figure 28. Optional Offset Nulling Circuit

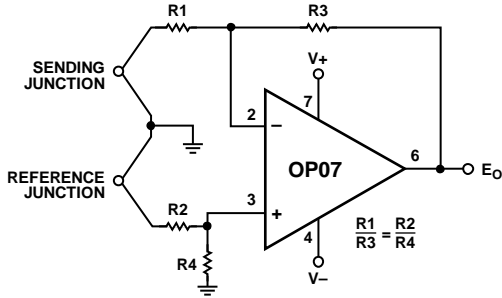
00316-028



NOTES  
1. PINOUT SHOWN FOR P PACKAGE

Figure 31. Adjustment-Free Precision Summing Amplifier

00316-031



NOTES  
1. PINOUT SHOWN FOR P PACKAGE

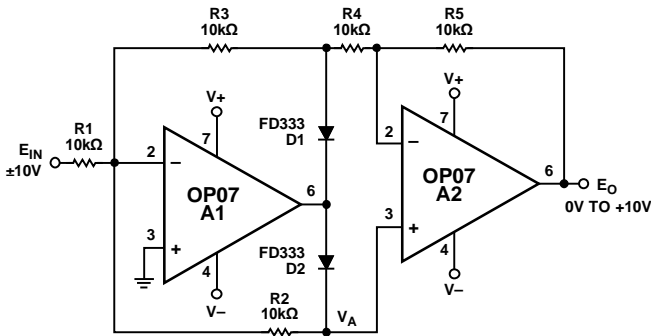
Figure 32. High Stability Thermocouple Amplifier

00316-032

**APPLICATIONS INFORMATION**

The OP07 provides stable operation with load capacitance of up to 500 pF and  $\pm 10$  V swings; larger capacitances should be decoupled with a 50  $\Omega$  decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation is obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

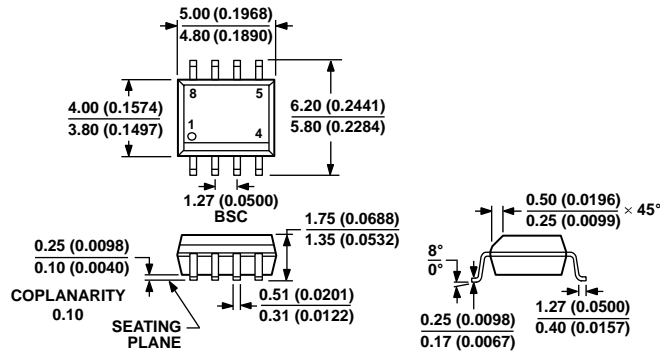


NOTES  
1. PINOUT SHOWN FOR P PACKAGE

Figure 33. Precision Absolute-Value Circuit

00316-033

OUTLINE DIMENSIONS

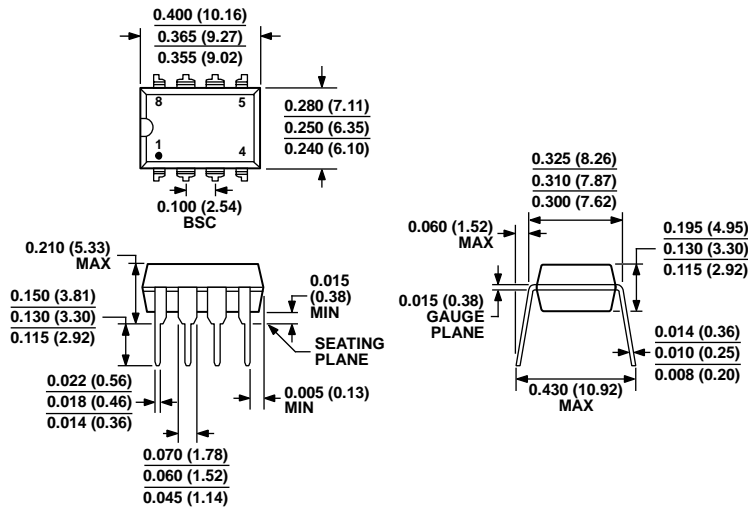


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 34. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body S-Suffix  
 (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.  
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

0770606-A

Figure 35. 8-Lead Plastic Dual-in-Line Package [PDIP]  
 P-Suffix  
 (N-8)

Dimensions shown in inches and (millimeters)

**ORDERING GUIDE**

<b>Model<sup>1</sup></b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>
OP07EPZ	0°C to 70°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CPZ	-40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CSZ	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**



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