



STP77N6F6

N-channel 60 V, 6.6 mΩ typ., 77 A STripFET™ VI DeepGATE™ Power MOSFET in a TO-220 package

Datasheet — production data

Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STP77N6F6	60 V	7.9 mΩ (V _{GS} =10 V)	77 A	80 W

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

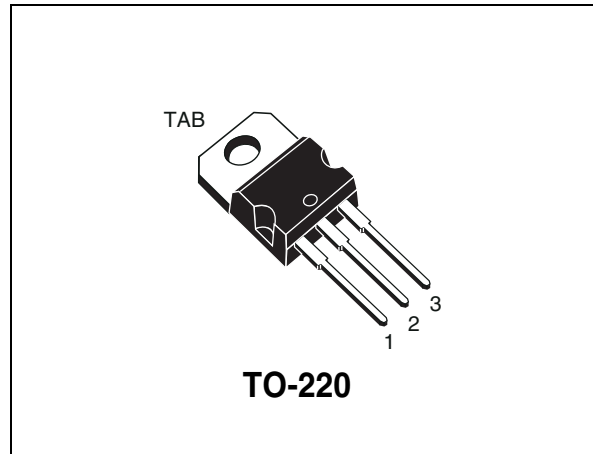


Figure 1. Internal schematic diagram

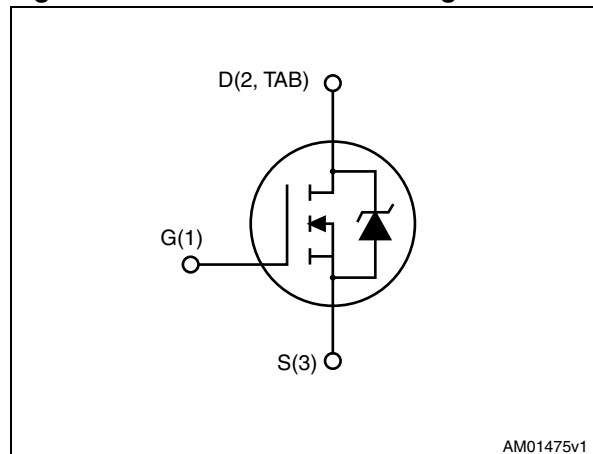


Table 1. Device summary

Order code	Marking	Package	Packaging
STP77N6F6	77N6F6	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	
$I_D^{(1)}$	Drain current (continuous) at $T_c = 25\text{ }^\circ\text{C}$	77	A
$I_D^{(1)}$	Drain current (continuous) at $T_c = 100\text{ }^\circ\text{C}$	55	
$I_{DM}^{(2)}$	Drain Current (pulsed)	308	
$P_{TOT}^{(1)}$	Total dissipation at $T_c = 25\text{ }^\circ\text{C}$	80	W
T_{JPstg}	Operating junction temperature storage temperature	-55 to 175	$^\circ\text{C}$

1. This value is rated according to R_{thj-c}
2. Pulse width is limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case	1.88	$^\circ\text{C}/\text{W}$
$R_{thj-a}^{(1)}$	Thermal resistance junction-ambient	62.5	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10$ sec

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by maximum junction temperature)	TBD	A
E_{AS}	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 14\text{ V}$)	TBD	mJ

2 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu A$	60			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 60\text{ V}$ $V_{DS} = 60\text{ V}, T_J = 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 33\text{ A}$		6.6	7.9	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			5300		
C_{oss}	Output capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1290	-	μF
C_{rss}	Reverse transfer capacitance			217		
Q_g	Total gate charge			76		
Q_{gs}	Gate-source charge	$V_{DD} = 30\text{ V}, I_D = 77\text{ A},$ $V_{GS} = 10\text{ V}$	-	TBD	-	nC
Q_{gd}	Gate-drain charge			TBD		
R_g	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3.6	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time		-		-	
t_r	Rise time	$V_{DD} = 30\text{ V}, I_D = 33\text{ A}$ $R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$		TBD		
$t_{d(off)}$	Turn-off-delay time		-		-	
t_f	Fall time					ns

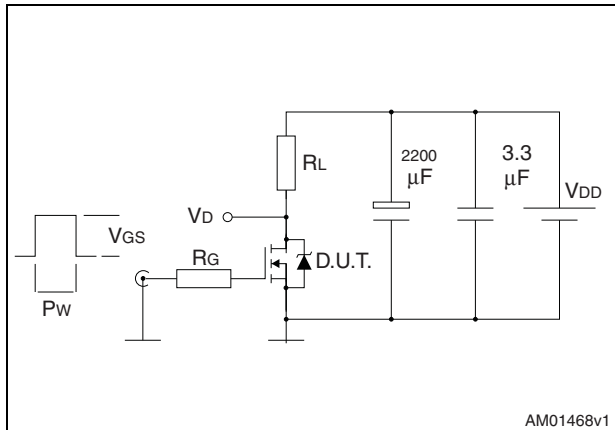
Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		77	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		308	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 77 \text{ A}, V_{GS} = 0$	-			V
t_{rr}	Reverse recovery time	$I_{SD} = 77 \text{ A}, V_{DD} = 80 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$ $T_j = 150 \text{ }^\circ\text{C}$	-	TBD	TBD	ns
Q_{rr}	Reverse recovery charge					nC
I_{RRM}	Reverse recovery current					A

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

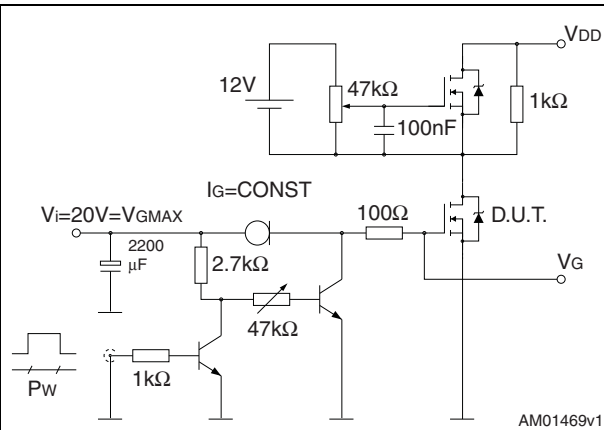
3 Test circuits

Figure 2. Switching times test circuit for resistive load



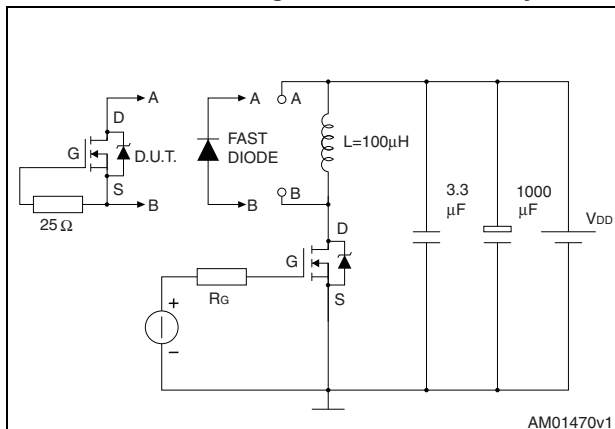
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Figure 3. Gate charge test circuit



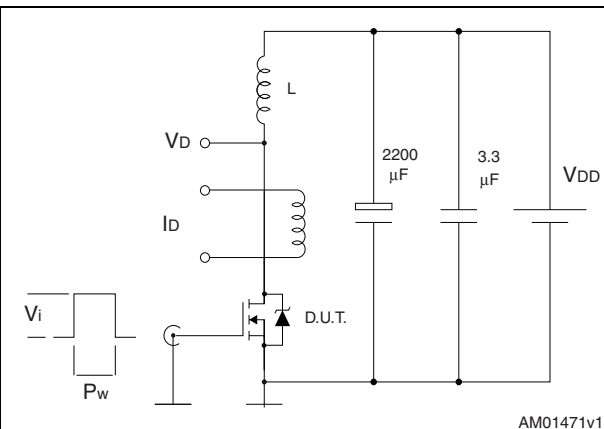
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Figure 4. Test circuit for inductive load switching and diode recovery times



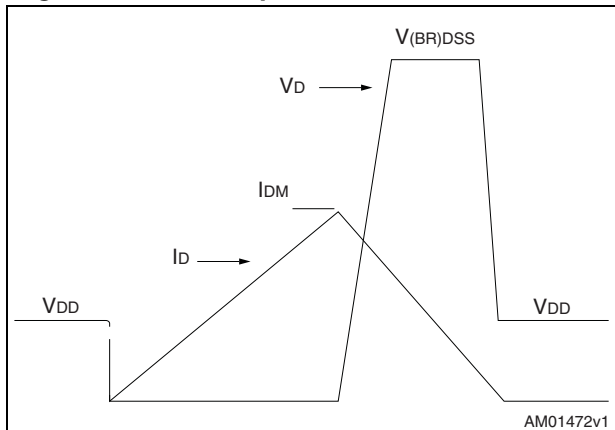
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Figure 5. Unclamped inductive load test circuit



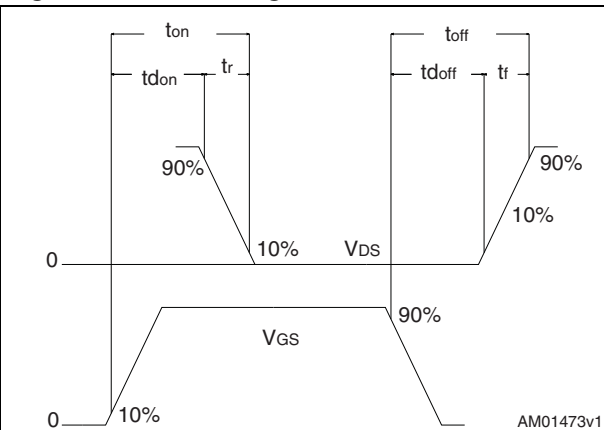
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



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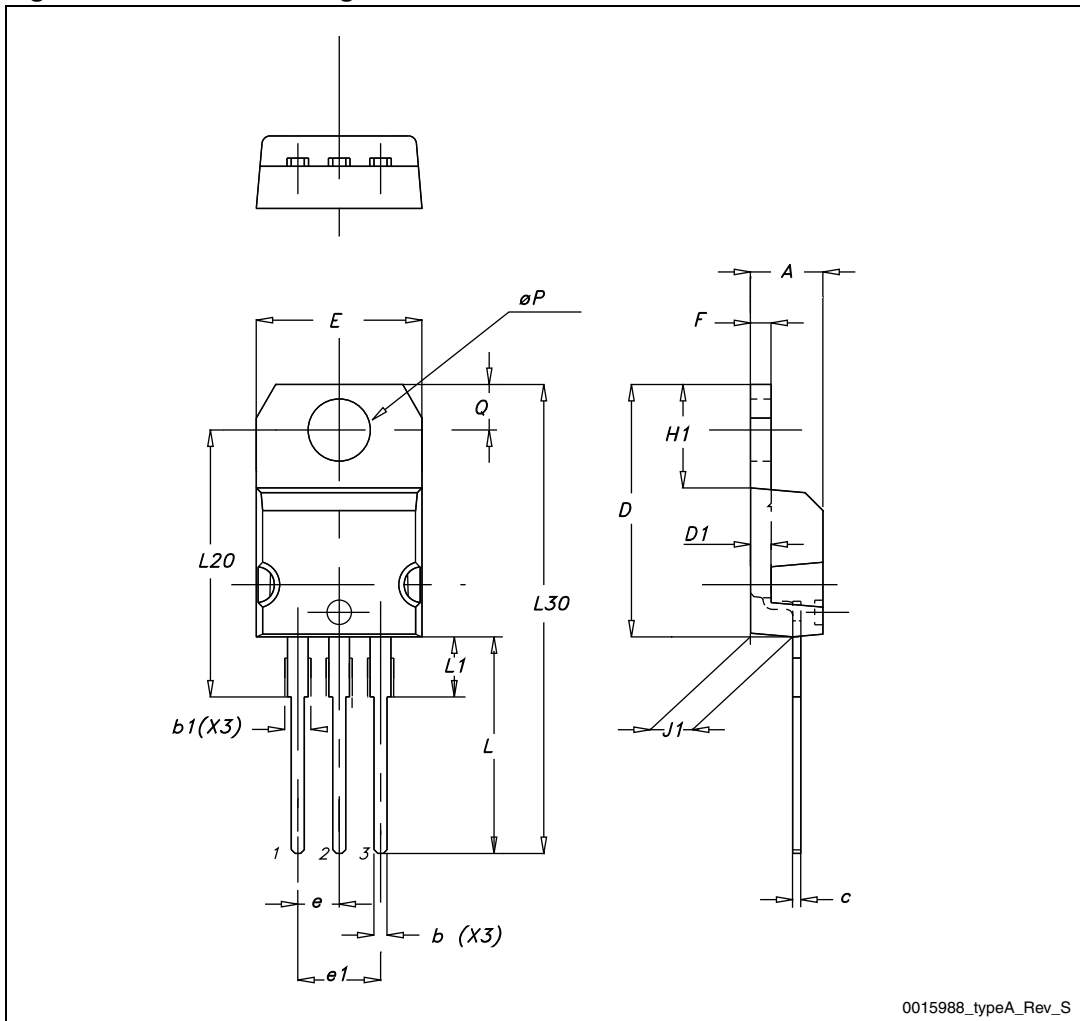
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 8. TO-220 drawing



0015988_typeA_Rev_S

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Dec-2012	1	First release.

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