

# MOSFET – P-Channel, POWERTRENCH®

**-150 V, -22 A, 53 mΩ**

## FDMS86263P

### General Description

This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

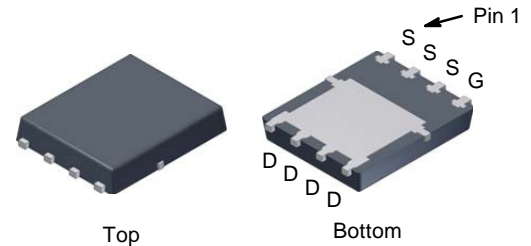
### Features

- Max  $r_{DS(on)}$  = 53 mΩ at  $V_{GS} = -10$  V,  $I_D = -4.4$  A
- Max  $r_{DS(on)}$  = 64 mΩ at  $V_{GS} = -6$  V,  $I_D = -4$  A
- Very Low  $R_{ds-on}$  in Mid-Voltage P-Channel Silicon Technology Optimized for Low  $Q_g$
- This Product is Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% Uil Tested
- This Device is Pb-Free and is RoHS Compliant

### Applications

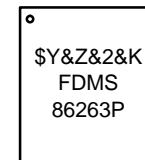
- Active Clamp Switch
- Load Switch

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
-150 V	53 mΩ @ -10 V	-22 A
	64 mΩ @ -6 V	



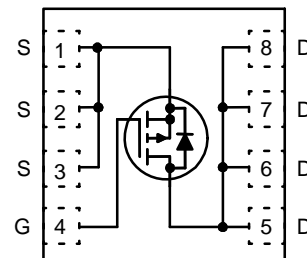
**PQFN8 5X6, 1.27P  
(Power 56)  
CASE 483AE**

### MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code Format
- &K = 2-Digits Lot Run Traceability Code
- FDMS86263P = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDMS86263P

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DS}$	Drain to Source Voltage	-150	V	
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V	
$I_D$	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 2a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	384	mJ	
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	104	W
	Power Dissipation (Note 2a)	$T_A = 25^\circ\text{C}$	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$	

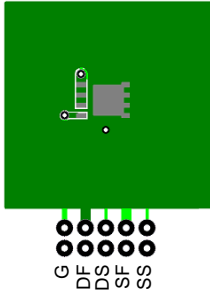
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Starting  $T_J = 25^\circ\text{C}$ ; P-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = -16\text{ A}$ ,  $V_{DD} = -150\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = -52\text{ A}$ .

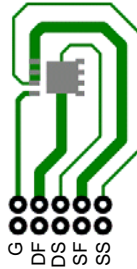
## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	50	

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $125^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	-116	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -120 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	7	-	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -4.4 A	-	42	53	mΩ
		V <sub>GS</sub> = -6 V, I <sub>D</sub> = -4 A	-	45	64	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -4.4 A, T <sub>J</sub> = 125°C	-	71	94	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -4.4 A	-	19	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2935	3905	pF
C <sub>oss</sub>	Output Capacitance		-	238	315	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	11	20	pF
R <sub>g</sub>	Gate Resistance		0.1	2.7	5.4	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -75 V, I <sub>D</sub> = -4.4 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω	-	17	31	ns
t <sub>r</sub>	Rise Time		-	10	21	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	37	59	ns
t <sub>f</sub>	Fall Time		-	14	25	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -10 V, V <sub>DD</sub> = -75 V, I <sub>D</sub> = -4.4 A	-	45	63	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -6 V, V <sub>DD</sub> = -75 V, I <sub>D</sub> = -4.4 A	-	29	40	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = -75 V, I <sub>D</sub> = -4.4 A	-	11.3	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	8.9	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -4.4 A (Note 3)	-	-0.79	-1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2 A (Note 3)	-	-0.75	-1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -4.4 A, di/dt = 100 A/μs	-	91	146	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	287	460	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

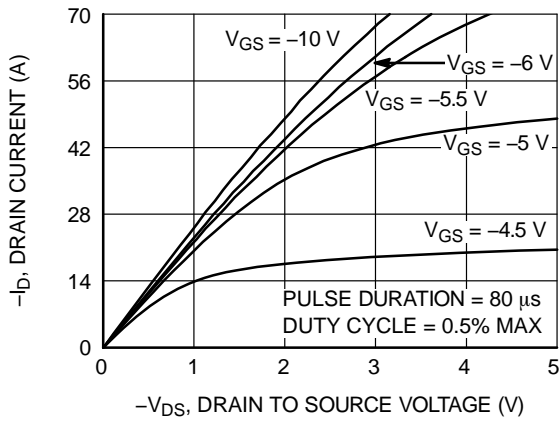


Figure 1. On Region Characteristics

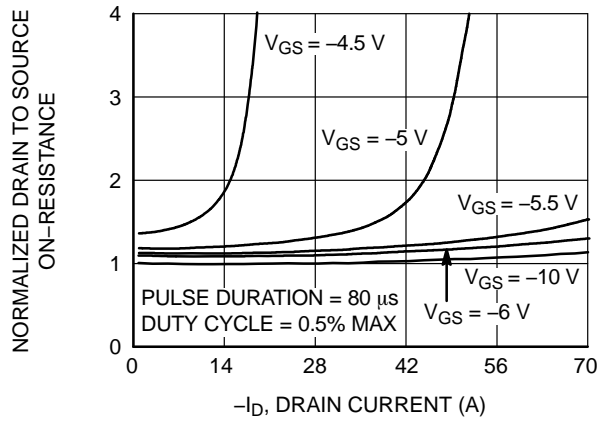


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

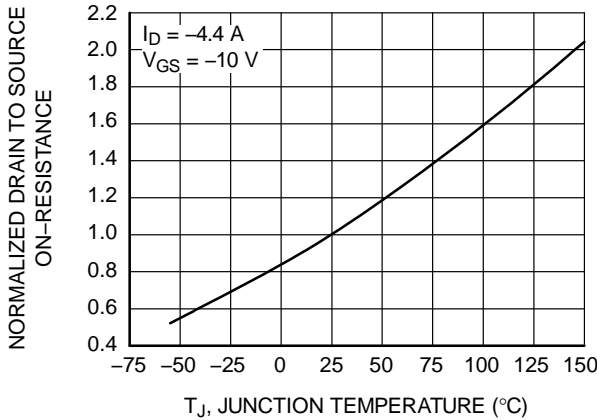


Figure 3. Normalized On-Resistance vs. Junction Temperature

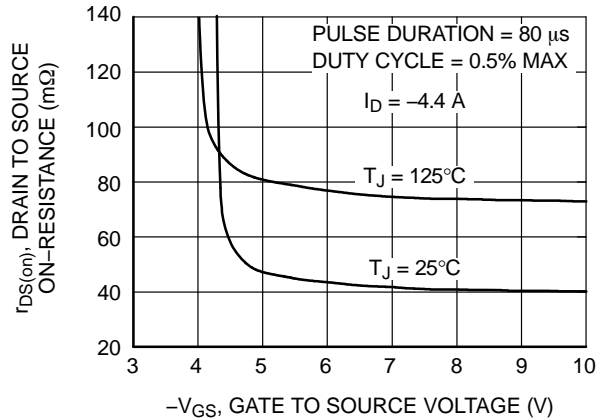


Figure 4. On-Resistance vs. Gate to Source Voltage

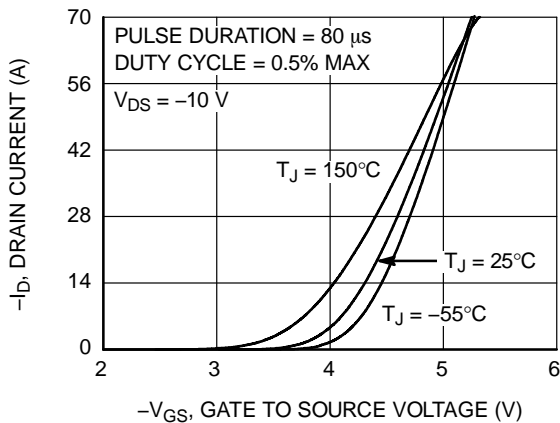


Figure 5. Transfer Characteristics

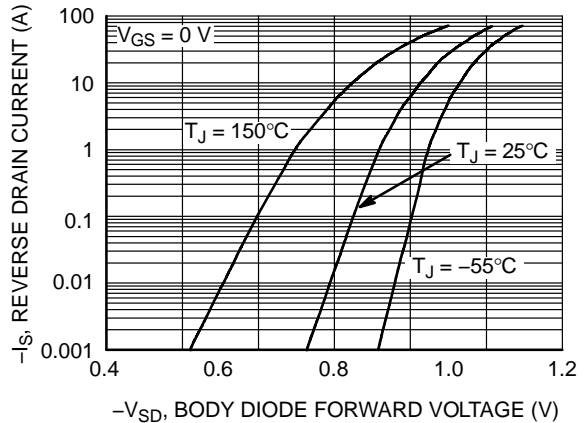


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

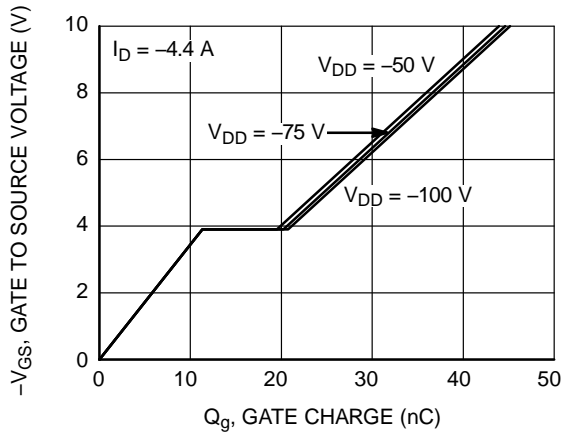


Figure 7. Gate Charge Characteristics

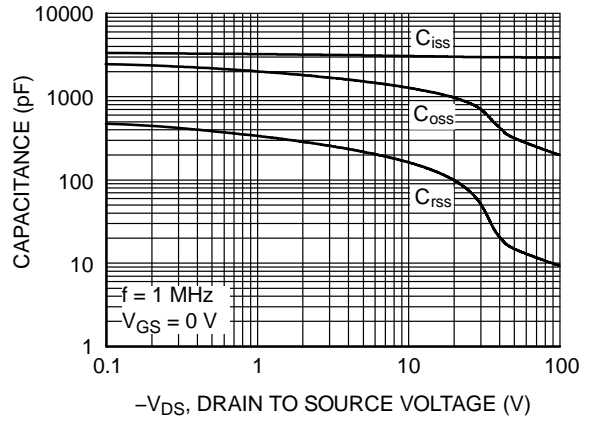


Figure 8. Capacitance vs. Drain to Source Voltage

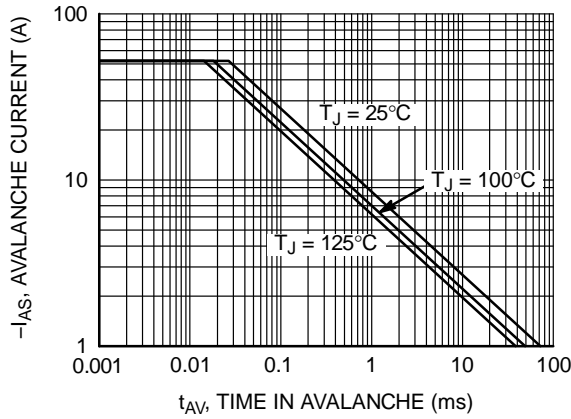


Figure 9. Unclamped Inductive Switching Capability

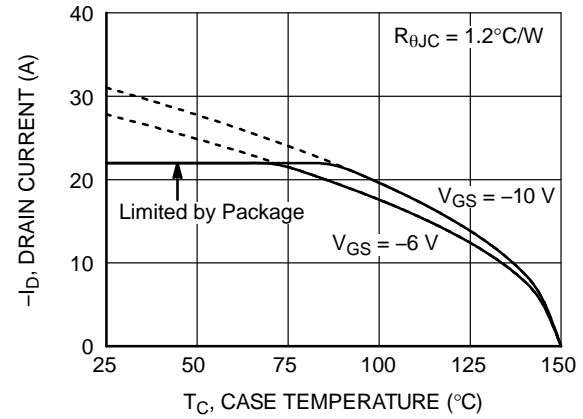


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

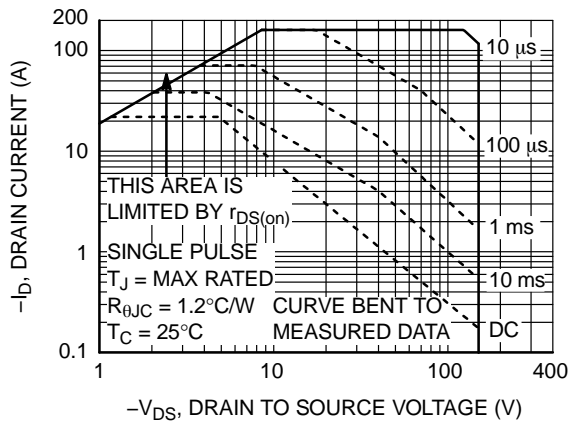


Figure 11. Forward Bias Safe Operating Area

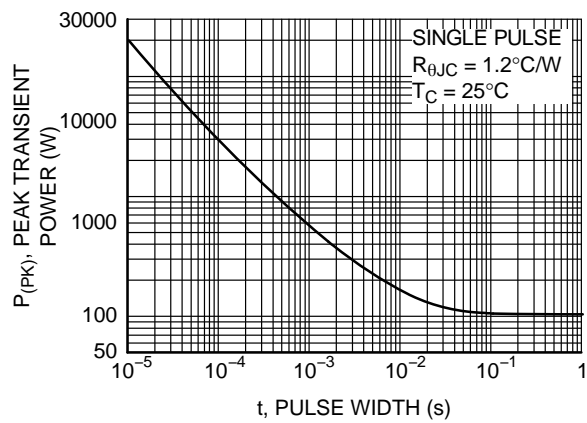


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

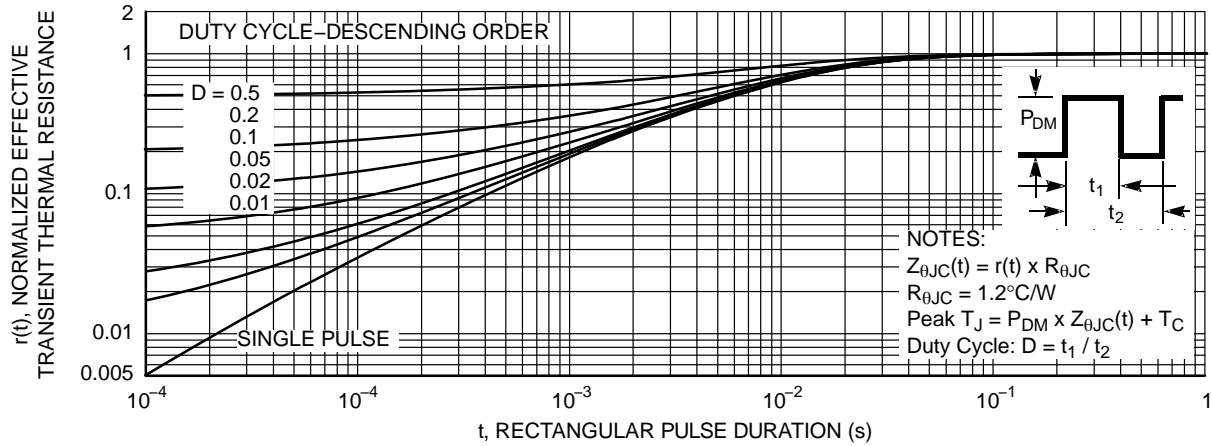
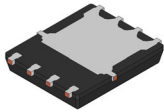


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

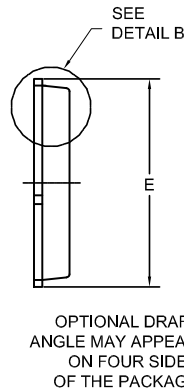
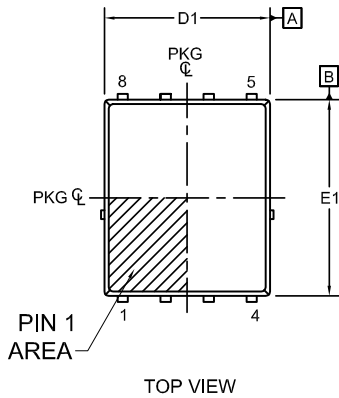
Device	Device Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMS86263P	FDMS86263P	PQFN8 5X6, 1.27P Power 56 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

<sup>†</sup>For Information On Tape And Reel Specifications, Including Part Orientation And Tape Sizes, Please Refer To Our Tape And Reel Packaging Specifications Brochure, Brd8011/D.



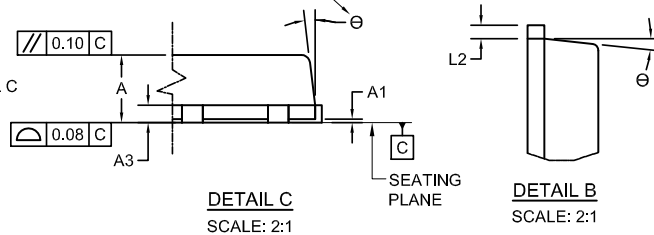
**PQFN8 5X6, 1.27P**  
CASE 483AE  
ISSUE C

DATE 21 JAN 2022

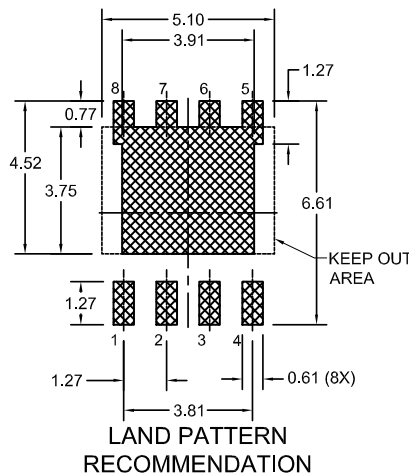
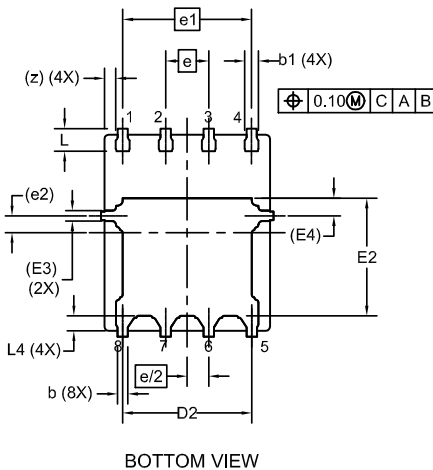


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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