

MOSFET – N-Channel, Shielded Gate, POWERTRENCH® 150 V, 62 A, 12.4 mΩ

FDMS86255

Description

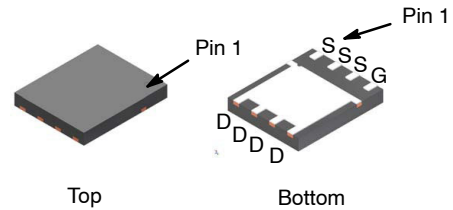
This N-Channel MOSFET is produced using **onsemi** advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

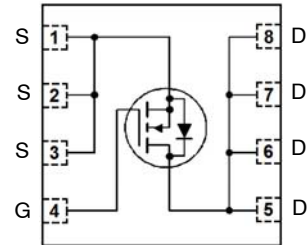
- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 12.4 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $R_{DS(on)}$ = 15.5 mΩ at $V_{GS} = 6$ V, $I_D = 8$ A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant
- These Device is Halogen Free

Applications

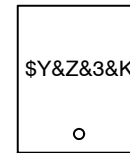
- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



PQFN8 5X6, 1.27P
CASE 483AG



MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Location
- &3 = Date Code (Year and Week)
- &K = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Unit
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous, $T_C = 25^\circ\text{C}$	62	A
	Continuous, $T_A = 25^\circ\text{C}$ (Note 1a)	10	
	Pulsed (Note 4)	271	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	541	mJ
P_D	Power Dissipation, $T_C = 25^\circ\text{C}$	113	W
	Power Dissipation, $T_A = 25^\circ\text{C}$ (Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	150	-	-	V
ΔBV_{DSS} ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	-	109	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}, V_{GS} = 0\ \text{V}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	-	-	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$\Delta V_{GS(th)}$ ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	-	-11	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}$	-	9.5	12.4	m Ω
		$V_{GS} = 6\ \text{V}, I_D = 8\ \text{A}$	-	11.5	15.5	
		$V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}, T_J = 125^\circ\text{C}$	-	19	25	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 10\ \text{A}$	-	35	-	S

DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	$V_{DS} = 75\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$	-	3200	4480	pF
C_{OOS}	Output Capacitance		-	291	410	pF
C_{rss}	Reverse Transfer Capacitance		-	11	20	pF
R_g	Gate Resistance		0.1	0.7	2.1	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}, I_D = 10\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$	-	21	34	ns	
t_r	Rise Time		-	4.5	10	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	28	45	ns	
t_f	Fall Time		-	6.2	12	ns	
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 75\ \text{V},$ $I_D = 10\ \text{A}$	-	45	63	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $6\ \text{V}$		-	29	41	nC

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ELECTRICAL CHARACTERISTICS (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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SWITCHING CHARACTERISTICS

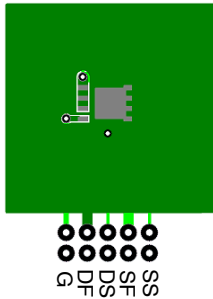
Q _{gs}	Gate to Source Charge		–	14	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	8.8	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

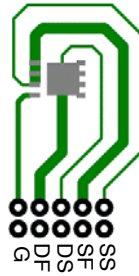
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.9 A (Note 2)	–	0.7	1.2	V
		V _{GS} = 0 V, I _S = 10 A (Note 2)	–	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 10 A, di/dt = 100 A/μs	–	87	139	ns
Q _{rr}	Reverse Recovery Charge		–	165	264	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 45°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 115°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E_{AS} of 541 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 19 A, V_{DD} = 150 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 60 A.
- Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

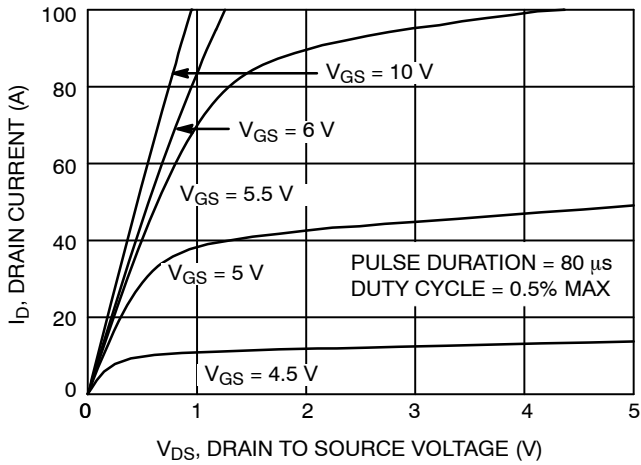


Figure 1. On-Region Characteristics

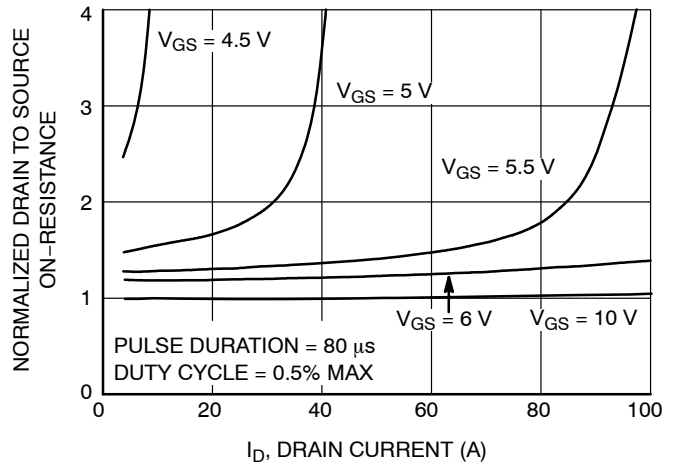


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

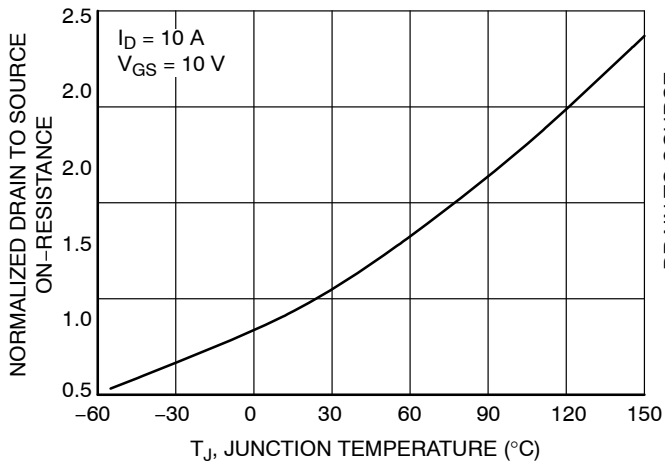


Figure 3. Normalized On-Resistance vs Junction Temperature

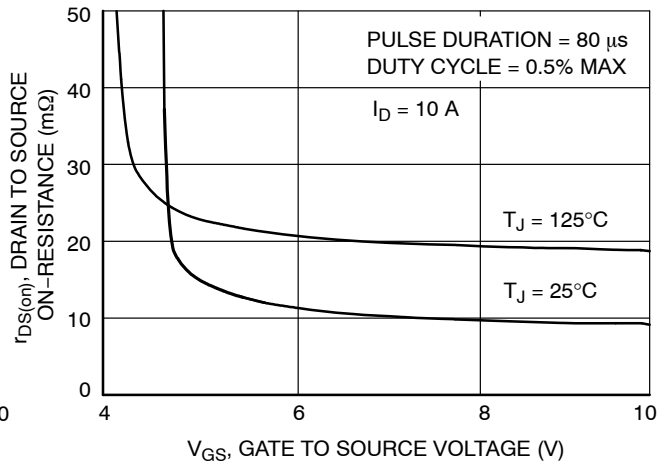


Figure 4. On-Resistance vs Gate to Source Voltage

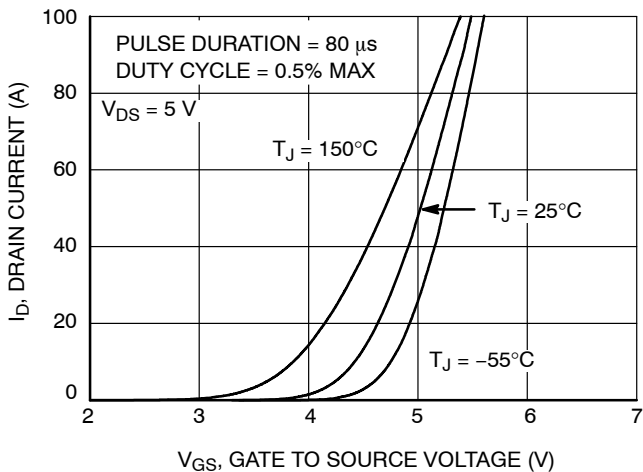


Figure 5. Transfer Characteristics

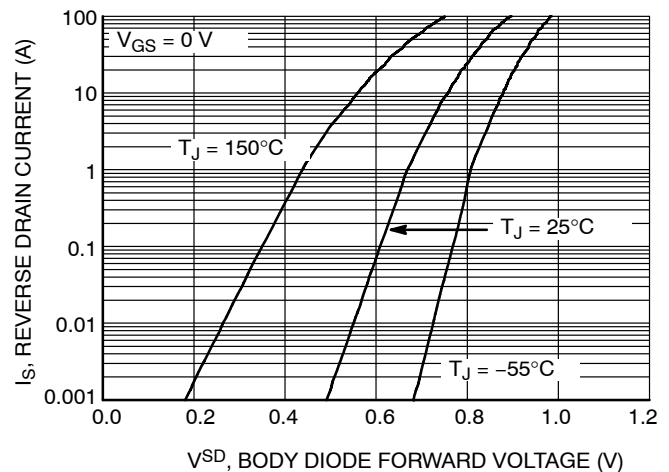


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued) $T_J = 25^\circ\text{C}$ unless otherwise noted

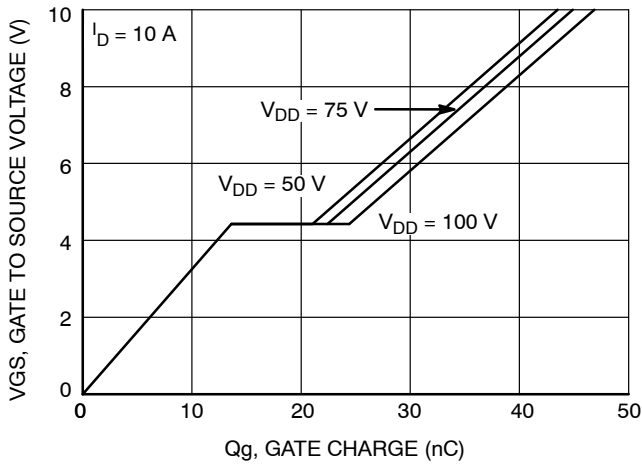


Figure 7. Gate Charge Characteristics

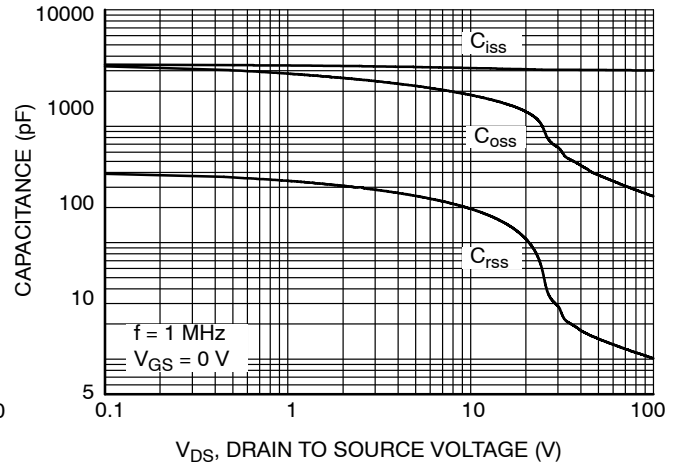


Figure 8. Capacitance vs Drain to Source Voltage

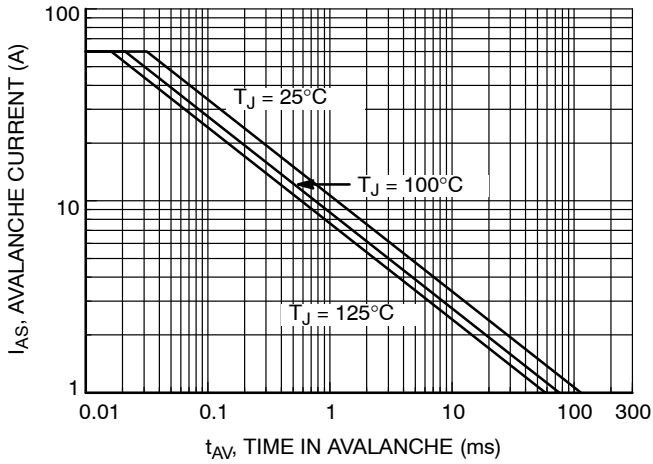


Figure 9. Unclamped Inductive Switching Capability

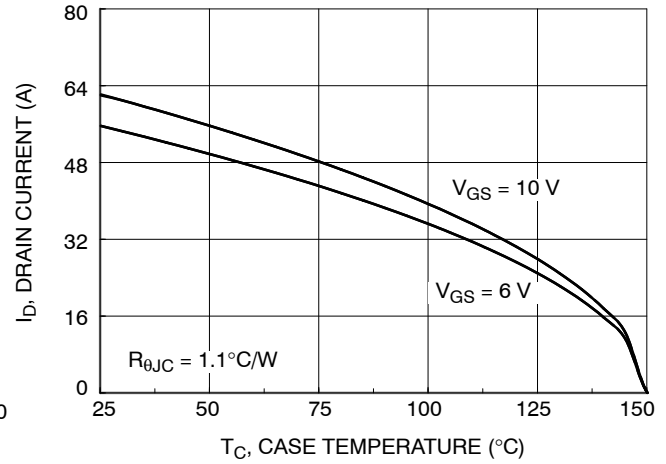


Figure 10. Maximum Continuous Drain Current vs Case Temperature

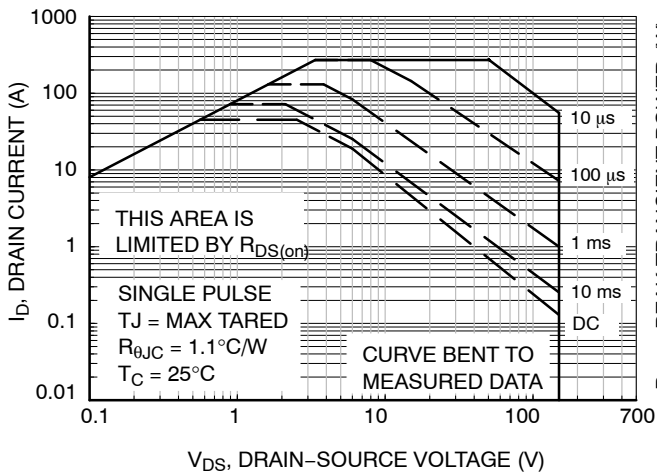


Figure 11. Forward Bias Safe Operating Area

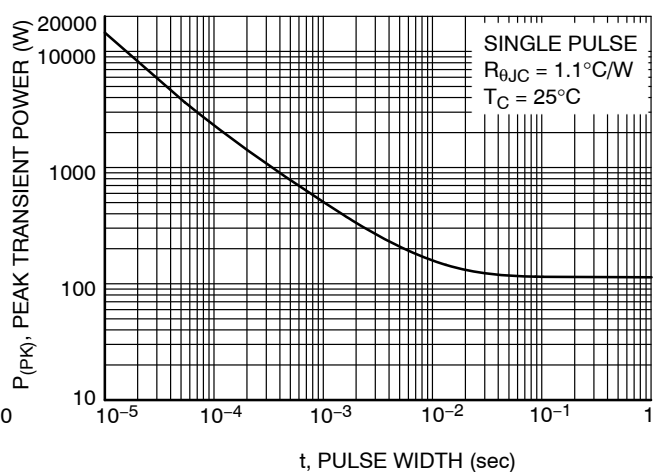


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued) $T_J = 25^\circ\text{C}$ unless otherwise noted

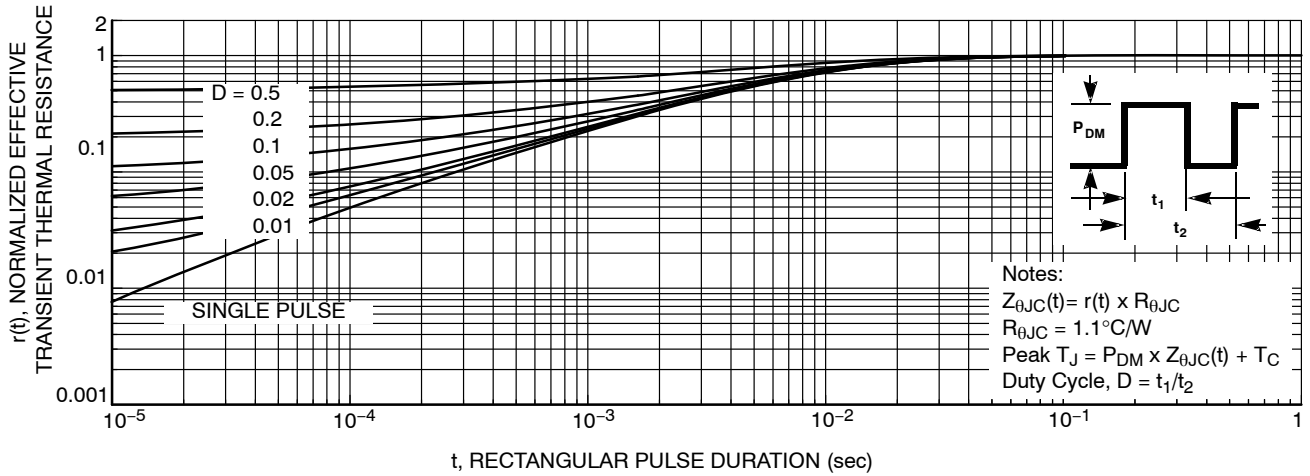


Figure 13. Transient Thermal Response Curve

ORDERING INFORMATION

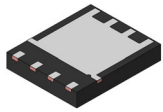
Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
FDMS86255	FDMS86255	PQFN8 (Halogen Free)	13"	12 mm	3000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

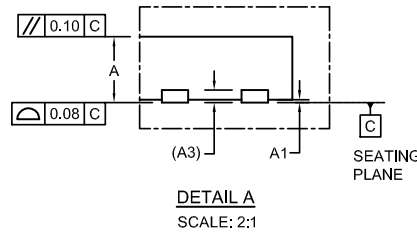
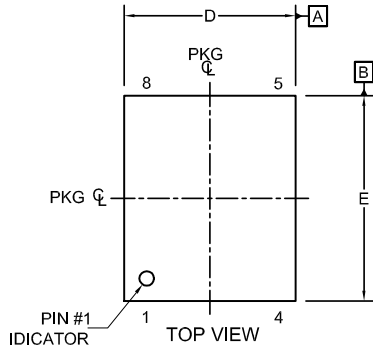
PACKAGE DIMENSIONS

ON Semiconductor®



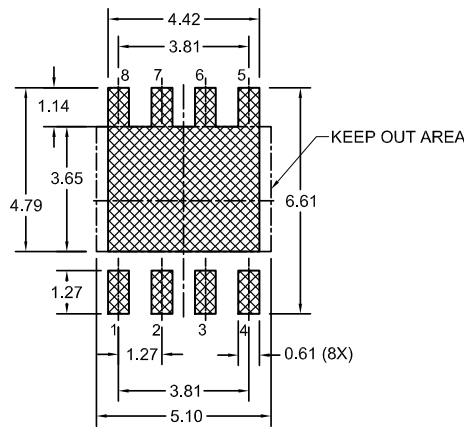
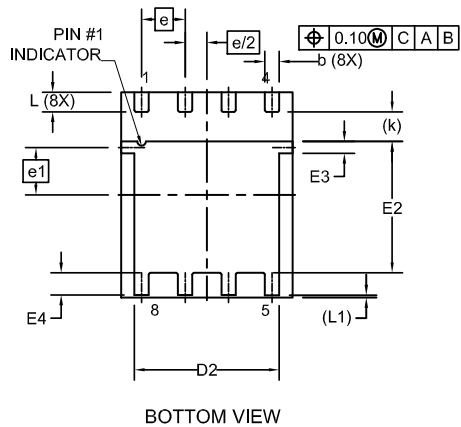
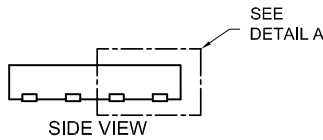
PQFN8 5X6, 1.27P CASE 483AG ISSUE A

DATE 25 JUN 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	3.74	3.84	3.94
E3	0.25	0.35	0.45
E4	0.60	0.70	0.80
e	1.27 BSC		
e/2	0.635 BSC		
e1	1.31 BSC		
k	0.86 REF		
L	0.47	0.57	0.67
L1	0.08REF		

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