

SNx4HC166 8-Bit Parallel-Load Shift Registers

1 Features

- Wide operating voltage range of 2V to 6V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80µA max I_{CC}
- Typical $t_{pd} = 13$ ns
- ±4mA output drive at 5V
- Low input current of 1µA max
- Synchronous load
- Direct overriding clear
- Parallel-to-serial conversion

2 Applications

Increase number of inputs/outputs to a microcontroller

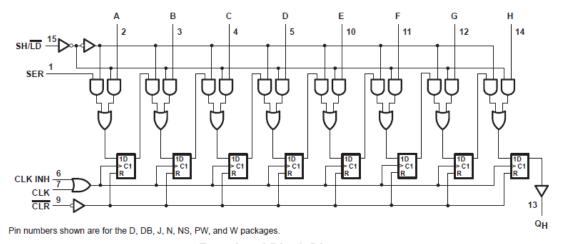
3 Description

The SNx4HC166 device contains an 8-bit shift register with one serial input and eight parallel-load inputs.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)(2)
	D (SOIC, 16)	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 5.30mm
SN74HC166	N (PDIP, 16)	19.31mm × 6.35mm
	NS (SOP, 16)	6.20mm × 5.30mm
	PW (TSSOP, 16)	5.00mm × 4.40mm
	J (CDIP, 16)	24.38mm × 6.92mm
SN54HC166	FK (LCCC, 20)	8.89mm × 8.45mm
	W (CFP, 16)	10.16mm × 6.73mm

- For more information, see Section 11.
- (2)The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

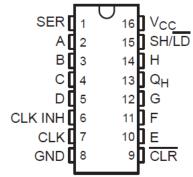


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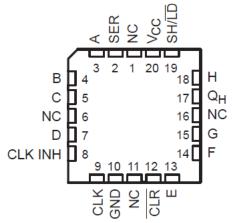
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4 Pin Configuration and Functions



J, D, DB, N, NS, or PW Package 16-Pin CDIP, SOIC, SSOP, PDIP, SO, TSSOP Top View



NC - No internal connection

FK Package 20-Pin LCCC Top View

Pin Functions

PIN		TYPE	DESCRIPTION			
NAME	NO. ⁽¹⁾	IIPE	DESCRIPTION			
SER	1	Input	Serial input			
Α	2	Input	Parallel input A			
В	3	Input	Parallel input B			
С	4	Input	Parallel input C			
D	5	Input	Parallel input D			
CLK INH	6	Input	Clock inhibit input			
CLK	7	Input	Clock input, positive edge triggered			
GND	8	_	Ground			
CLR	9	Input	Clear input, active low			
E	10	Input	Parallel input E			
F	11	Input	Parallel input F			
G	12	Input	Parallel input G			
Q _H	13	Output	Q _H output			
Н	14	Input	Parallel input H			
SH/ LD	15	Input	Shift/ load input, enable shifting when input is high, load data when input is low			
V _{CC}	16	_	Positive supply			

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	Supply voltage range		7	V
I _{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC}	or GND		±50	mA
TJ	Junction temperature	Junction temperature			°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			SN	54HC166		SN74HC166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
V _{CC}	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2V	1.5			1.5			
V _{IH} High-level input voltage	V _{CC} = 4.5V	3.15			3.15			V	
		V _{CC} = 6V	4.2			4.2			
	V _{CC} = 2V			0.5			0.5		
V _{IL}	Low-level input voltage	V _{CC} = 4.5V			1.35			1.35	V
		V _{CC} = 6V			1.8			1.8	
VI	Input voltage		0		V _{CC}	0		V _{CC}	V
Vo	Output voltage		0		V _{CC}	0		V _{CC}	V
		V _{CC} = 2V			1000			1000	
$\Delta t/\Delta v^{(2)}$	Δt/Δv ⁽²⁾ Input transition rise/fall time	V _{CC} = 4.5V			500			500	ns
		V _{CC} = 6V			400			400	
T _A	Operating free-air temperatu	re	-55		125	-55		125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
THERMAL METRIC		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	73	82	67	64	108	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	TEST		T _A = 25°C		SN54HC	166	SN74HC166			
PARAMETER	CONDITIONS(1)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2	1.9	1.998		1.9		1.9		
	I _{OH} = −20μA	4.5	4.4	4.499		4.4		4.4		
V _{OH}		6	5.9	5.999		5.9		5.9		V
	I _{OH} = -4mA	4.5	3.98	4.3		3.7		3.7		
	I _{OH} = −5.2mA	6	5.48	5.8		5.2		5.2		
		2		0.002	0.1		0.1		0.1	
	I _{OL} = 20μA	4.5		0.001	0.1		0.1		0.1	
V _{OL}		6		0.001	0.1		0.1		0.1	V
	I _{OL} = 4mA	4.5		0.17	0.26		0.4		0.4	
	I _{OL} = 5.2mA	6		0.15	0.26		0.4		0.4	
I ₁	$V_I = V_{CC}$ or 0	6		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0, I_O = 0	6			8		160		160	μΑ
Ci		2 to 6		3	10		10		10	pF

⁽¹⁾ $V_I = V_{IH}$ or V_{IL} , unless otherwise noted.



5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V 00	T _A = 2	5°C	SN54H0	2166	SN74HC	166	LINUT
			V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2		6		4.2		5	
f_{clock}	Clock frequence	су	4.5		31		21		25	MHz
			6		36		25		29	
			2	100		150		125		
		CLR low	4.5	20		30		25		
+	Dulas duration		6	17		26		21		no
t _w	Pulse duration		2	80		120		100		ns
		CLK high or low	4.5	16		24		20		
			6	14		20		17		
			2	145		220		180		
		SH/LD high before CLK↑	4.5	29		44		36		
			6	25		38		31		
			2	80		120		100		
		SER before CLK↑	4.5	16		24		20		
			6	14		20		17		
			2	100		150		125		
t _{su}	Setup time	CLK INH low before CLK↑	4.5	20		30		25		ns
			6	17		26		21		
			2	80		120		100		
		Data before CLK↑	4.5	16		24		20		
			6	14		20		17		
			2	40		60		50		
		CLR inactive before CLK↑	4.5	8		12		10		
			6	7		10		9		
			2	0		0		0		
		SH/LD high after CLK↑	4.5	0		0		0		
			6	0		0		0		
			2	5		5		5		
		SER after CLK↑	4.5	5		5		5		
ŧ.	Hold time		6	5		5		5		nc
t _h	Hold time	ine	2	0		0		0		ns
		CLK INH high after CLK↑	4.5	0		0		0		
			6	0		0		0		
			2	5		5		5		
		Data after CLK↑	4.5	5		5		5		
			6	5		5		5		

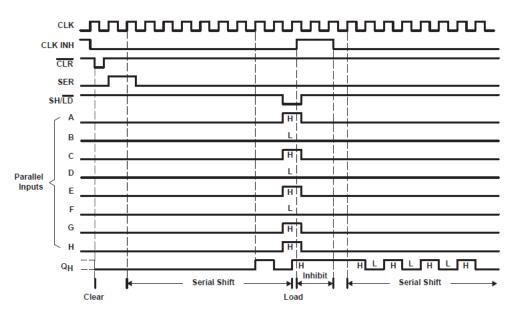


Figure 5-1. Typical Clear, Shift, Load, Inhibit, and Shift Sequence

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50pF (unless otherwise noted) (see Figure 6)

PARAMETER	FROM	то	V 00	T _A = 25°C			SN54H0	C166	SN74HC166		UNIT	
FARAIVIETER	(INPUT)	(OUTPUT)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT	
			2	6	11		4.2		4.2			
f _{max}			4.5	31	36		21		21		MHz	
			6	36	45		25		25			
			2		62	120		180		180		
t _{PHL}	CLR	CLR	Q _H	4.5		18	24		36		36	ns
			6		13	20		31		31		
			2		75	150		225		225		
t _{pd}	CLK	Q _H	4.5		15	30		45		45	ns	
			6		13	26		38		38		
			2		38	75		110		110		
t _t		Any	4.5		8	15		22		22	ns	
			6		6	13		19		19		

5.7 Operating Characteristics

T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

6 Parameter Measurement Information

 t_{pd} is the maximum between t_{PLH} and t_{PHL}

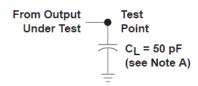


Figure 6-1. Load Circuit

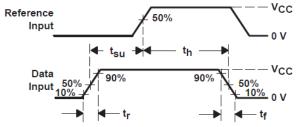


Figure 6-3. Voltage Waveforms
Setup and Hold and Input Rise and Fall Times

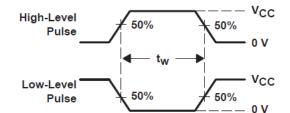


Figure 6-2. Voltage Waveforms
Pulse Durations

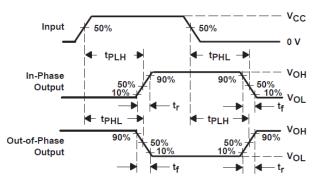


Figure 6-4. Voltage Waveforms
Propagation Delay and Output Transition Times

- A. C_L includes probe and jig capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following charactersitics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_f = 6$ ns, $t_f = 6$ ns.
- C. For clock inputs, f_{max} is measured when the input duty cycle is 50%
- D. The outputs are measured one at a time with one input transition per measurement.

7 Detailed Description

7.1 Overview

The SNx4HC166 is a parallel-load 8-bit shift register with asynchronous clear ($\overline{\text{CLR}}$). This parallel-in or serial-in, serial-out shift register features gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the mode select (SH/ $\overline{\text{LD}}$) input. When high, SH/ $\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (A through H) data inputs are enabled, and synchronous loading occurs on the next clock pulse.

During parallel loading, serial data flow is inhibited. Clocking is accomplished on the rising edge of CLK or CLK INH, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. CLK INH should be changed to the high level only when CLK is high.

CLR overrides all other inputs, including CLK, and resets all flip-flops to zero.

7.2 Functional Block Diagram

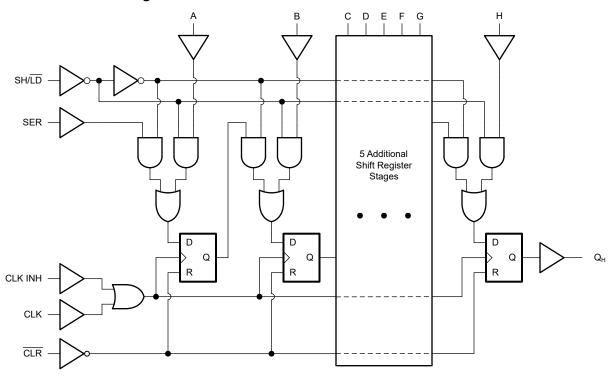


Figure 7-1. Logic Diagram (Positive Logic) for SNx4HC166

7.3 Feature Description

7.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.



Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a $10k\Omega$ resistor, however, is recommended and will typically meet all requirements.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a $10k\Omega$ resistor is recommended and typically will meet all requirements.

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7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4HC166.

Table 7-1. Operating Mode Table

	INPUTS ⁽¹⁾						
SH/LD	CLK	CLK INH	FUNCTION				
L	Х	X	Parallel load ⁽²⁾				
Н	Н	X	No change				
Н	Х	Н	No change				
Н	L	1	Shift ⁽³⁾				
Н	1	L	Shift ⁽³⁾				

- (1) H = High voltage level, L = Low voltage level, X = Don't care, ↑ = Low to high transition
- (2) Parallel load: Values at inputs A through H are loaded to respective internal registers synchronously with the clock.
- (3) Shift: Content of each internal register shifts towards serial output Q_H synchronously with the clock. Data at SER is shifted into the first register.

Table 7-2. Output Function Table

INTERNAL RE	OUTPUTS(3)	
A — G	Н	Q
X	L	L
X	Н	Н

- Internal registers refer to the shift registers inside the device.
 These values are set by loading data from the parallel or serial inputs.
- (2) H = High voltage level, L = Low voltage level, X = Don't care
- (3) H = Driving high, L = Driving low

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SNx4HC166 is used to increase the number of inputs on a microcontroller. Unlike other I/O expanders, the SNx4HC166 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

At power-up, the initial states of the internal shift registers are unknown. To give them a defined state of zero, the device can be cleared by applying a low signal to the clear (\overline{CLR}) input. Alternatively, data can be loaded in directly by switching to load mode $(SH/\overline{LD} = low)$, then pulsing the clock (CLK) input once.

8.2 Typical Application

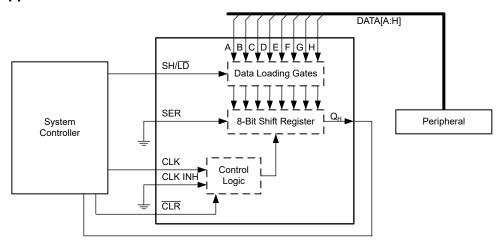


Figure 8-1. Typical Application Block Diagram

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4HC166 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4HC166 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SNx4HC166 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4HC166 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A $10k\Omega$ resistor value is often used due to these factors.

The SNx4HC166 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
- 2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4HC166 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

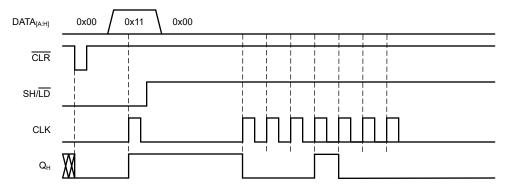


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SNx4HC166, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.



8.4.2 Layout Example

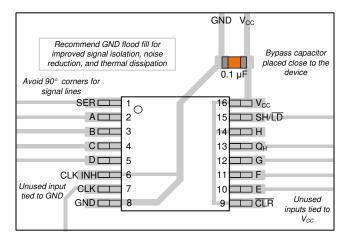


Figure 8-3. Example Layout for the SNx4HC166



9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

 Added applications Updated SN74HC166 operating temperature to 125°C and respective values in Recommended Operating Conditionstable, Electrical Characteristics table, and Switching Characteristics table 	CI	hanges from Revision E (February 2022) to Revision F (May 2025)	Page
 Updated SN74HC166 operating temperature to 125°C and respective values in Recommended Operating Conditionstable, Electrical Characteristics table, and Switching Characteristics table. 	•	Added applications	1
, , , , , , , , , , , , , , , , , , ,	•		
		Conditionstable, Electrical Characteristics table, and Switching Characteristics table	1
Added Pin Functions table and Application and Implementation section	•	Added Pin Functions table and Application and Implementation section	1

Changes from Revision D (December 1982) to Revision E (February 2022)

Pag

 Updated the numbering, formatting, tables, figures, and cross-references thorughout the document to reflect modern data sheet standards......



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9050101Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
5962-9050101QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101QE A SNJ54HC166J
5962-9050101VEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101VE A SNV54HC166J
5962-9050101VEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101VE A SNV54HC166J
SN54HC166J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC166J
SN54HC166J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC166J
SN74HC166D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HC166DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DRE4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166DRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC166N
SN74HC166N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC166N
SN74HC166NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HC166PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166



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SNJ54HC166J



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Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74HC166PWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC166
SN74HC166PWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HC166
SN74HCS166DYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS166
SN74HCS166DYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS166
SNJ54HC166FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
SNJ54HC166FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9050101Q2A SNJ54HC 166FK
SNJ54HC166J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101Q A SNJ54HC166J
SNJ54HC166J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9050101Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC166, SN54HC166-SP, SN74HC166:

Catalog: SN74HC166, SN54HC166

Military: SN54HC166

Space: SN54HC166-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC166DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC166DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC166NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC166NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC166PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC166PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS166DYYR	SOT-23- THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3



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*All dimensions are nominal

All difficultions are florillial							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC166DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74HC166DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166DRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC166NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC166NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC166PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC166PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HCS166DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9050101Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC166N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC166N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC166FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC166FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA



SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AA



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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