

SN74LVC828A 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS347H-MARCH 1994-REVISED MARCH 2005

| FEATURES | DB, DGV, DW, NS, OR PW PACKAGE |
|---|--|
| Operates From 1.65 V to 3.6 V | (TOP VIEW) |
| Inputs Accept Voltages to 5.5 V | ┛────┣… |
| Max t_{pd} of 6.7 ns at 3.3 V | OE1 1 24 V _{CC} A1 2 23 Y1 |
| Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C | AT U 2 23 11 A2 [3 22] Y2 A3 [4 21] Y3 |
| Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C | A4 [5 20] Y4 A5 [6 19] Y5 |
| Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC}) | A6 [7 18] Y6 A7 [8 17] Y7 A8 [9 16] Y8 |
| I_{off} Supports Partial-Power-Down Mode Operation | A9 0 10 15 Y9 A10 11 14 Y10 |
| Latch-Up Performance Exceeds 250 mA Per JESD 17 | GND [12 13] OE2 |

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC828A provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable (OE1 or OE2) input is high, all ten outputs are in the high-impedance state. The SN74LVC828A provides inverting data at its outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

| T _A | PA | CKAGE ⁽¹⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING | | |
|----------------|-------------|----------------------|-----------------------|------------------|--|--|
| | | Tube of 25 | SN74LVC828ADW | 1.1/00004 | | |
| | SOIC – DW | Reel of 2000 | SN74LVC828ADWR | LVC828A | | |
| | SOP – NS | Reel of 2000 | SN74LVC828ANSR | LVC828A | | |
| 4000 to 0500 | SSOP – DB | Reel of 2000 | SN74LVC828ADBR | LC828A | | |
| –40°C to 85°C | | Tube of 60 | SN74LVC828APW | | | |
| | TSSOP – PW | Reel of 2000 | SN74LVC828APWR | LC828A | | |
| | | Reel of 250 | SN74LVC828APWT | | | |
| | TVSOP – DGV | Reel of 2000 | SN74LVC828ADGVR | LC828A | | |

ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

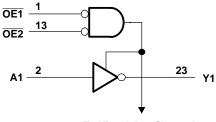
SN74LVC828A 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS347H-MARCH 1994-REVISED MARCH 2005

FUNCTION TABLE

| Ī | | INPUTS | OUTPUT | |
|---|-----|-----------|--------|---|
| | OE1 | DE1 OE2 A | | Y |
| Ī | L | L | L | Н |
| | L | L | Н | L |
| | н | Х | Х | Z |
| | Х | Н | Х | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



To Nine Other Channels

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT | |
|------------------|--|--|------|-----------------------|------|--|
| V _{CC} | Supply voltage range | | -0.5 | 6.5 | V | |
| VI | Input voltage range ⁽²⁾ | | -0.5 | 6.5 | V | |
| Vo | Voltage range applied to any output in the h | high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V | |
| Vo | Voltage range applied to any output in the h | high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V ₁ < 0 | | -50 | mA | |
| I _{OK} | Output clamp current | V ₀ < 0 | | -50 | mA | |
| I _O | Continuous output current | | ±50 | mA | | |
| | Continuous current through V_{CC} or GND | | | ±100 | mA | |
| | | DB package | | 63 | | |
| | | DGV package | | 86 | | |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DW package | | 46 | °C/W | |
| | | NS package | | 65 | | |
| | | PW package | | 88 | | |
| T _{stg} | Storage temperature range | | -65 | 150 | °C | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------------|------------------------------------|--|---------------------|----------------------|------------|
| V | Cupply voltage | Operating | 1.65 | 3.6 | V |
| V _{CC} | Supply voltage | Data retention only | 1.5 | | v |
| | | V _{CC} = 1.65 V to 1.95 V | $0.65 	imes V_{CC}$ | | |
| VIH | High-level input voltage | V_{CC} = 2.3 V to 2.7 V | 1.7 | | V |
| | | V_{CC} = 2.7 V to 3.6 V | 2 | | |
| | | V _{CC} = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | |
| VIL | Low-level input voltage | V_{CC} = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | | 0.8 | |
| VI | Input voltage | | 0 | 5.5 | V |
| V | / _O Output voltage | High or low state | 0 | V _{CC} | V |
| vo | | 3-state | 0 | 5.5 | v |
| | Output voltage | V _{CC} = 1.65 V | | -4 | |
| | High lovel output ourrent | $V_{CC} = 2.3 V$ | | -8 | س ۸ |
| I _{OH} | High-level output current | $V_{CC} = 2.7 V$ | | -12 | mA |
| | | $V_{CC} = 3 V$ | | -24 | |
| | | V _{CC} = 1.65 V | | 4 | |
| | Low level output ourrept | $V_{CC} = 2.3 V$ | | 8 | mA |
| I _{OL} | Low-level output current | $V_{CC} = 2.7 V$ | | 12 | |
| | | $V_{CC} = 3 V$ | | 24 | |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| T _A | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC828A **10-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS

SCAS347H-MARCH 1994-REVISED MARCH 2005

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST C | ONDITIONS | V _{cc} | MIN | TYP ⁽¹⁾ | MAX | UNIT | | |
|------------------|---|---------------------------------|-----------------|----------------|--------------------|------|------|--|--|
| | I _{OH} = −100 μA | | 1.65 V to 3.6 V | $V_{CC} - 0.2$ | | | | | |
| | I _{OH} = -4 mA | | 1.65 V | 1.2 | | | | | |
| | I _{OH} = -8 mA | | 2.3 V | 1.7 | | | v | | |
| V _{OH} | L _ 12 mA | | 2.7 V | 2.2 | | | V | | |
| | I _{OH} = -12 mA | | 3 V | 2.4 | | | | | |
| | I _{OH} = -24 mA | | 3 V | 2.2 | | | | | |
| | I _{OL} = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | | | |
| | $I_{OL} = 4 \text{ mA}$ | | 1.65 V | | | 0.45 | | | |
| V _{OL} | I _{OL} = 8 mA | | 2.3 V | | | 0.7 | V | | |
| | I _{OL} = 12 mA | | 2.7 V | | | 0.4 | | | |
| | I _{OL} = 24 mA | | 3 V | | | 0.55 | | | |
| I _I | V _I = 0 to 5.5 V | | 3.6 V | | | ±5 | μA | | |
| l _{off} | $V_{I} \text{ or } V_{O} = 5.5 \text{ V}$ | | 0 | | | ±10 | μA | | |
| I _{OZ} | $V_0 = 0$ to 5.5 V | | 3.6 V | | | ±10 | μA | | |
| | $V_I = V_{CC}$ or GND | | 2.6.1/ | | | 10 | ۸ | | |
| I _{CC} | $3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(2)}$ | $I_{O} = 0$ | 3.6 V | | | 10 | μA | | |
| ΔI_{CC} | One input at V _{CC} – 0.6 V, | Other inputs at V_{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA | | |
| Ci | $V_I = V_{CC}$ or GND | | 3.3 V | | 5 | | pF | | |
| Co | $V_{O} = V_{CC}$ or GND | | 3.3 V | | 7 | | pF | | |

All typical values are at V_{CC} = 3.3 V, T_A = 25^{\circ}C. This applies in the disabled state only. (1)

(2)

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | V _{CC} = 1.8 V ± 0.15 V | | V_{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V_{CC} = 3.3 V ± 0.3 V | |
|--------------------|-----------------|----------------|-----|-------------------------------------|-----|-----------------------------|-----|-------------------------|-----|-----------------------------|----|
| | (INFUT) | (001201) | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | А | Y | (1) | (1) | (1) | (1) | | 7.1 | 1 | 6.7 | ns |
| t _{en} | OE | Y | (1) | (1) | (1) | (1) | | 8.5 | 1 | 7.3 | ns |
| t _{dis} | OE | Y | (1) | (1) | (1) | (1) | | 7.3 | 1.8 | 6.7 | ns |
| t _{sk(o)} | | | | | | | | | | 1 | ns |

(1) This information was not available at the time of publication.

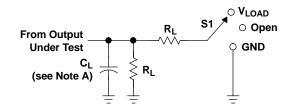
Operating Characteristics

 $T_A = 25^{\circ}C$

| | PARAMETER | | TEST | V _{CC} = 1.8 V | V_{CC} = 2.5 V | V_{CC} = 3.3 V | UNIT | |
|-----------------|-------------------------------|------------------|------------|-------------------------|------------------|------------------|------|--|
| | | CONDITIONS | TYP | TYP | TYP | | | |
| 6 | Power dissipation capacitance | Outputs enabled | f 10 MU | (1) | (1) | 24 | pF | |
| C _{pd} | per buffer/driver | Outputs disabled | f = 10 MHz | (1) | (1) | 7 | | |

(1) This information was not available at the time of publication.

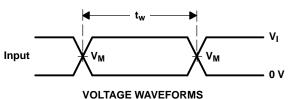
PARAMETER MEASUREMENT INFORMATION



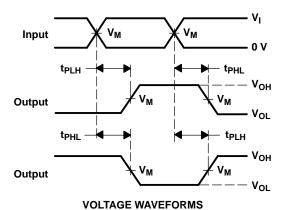
LOAD CIRCUIT

| TEST | S1 |
|------------------------------------|-------------------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | V _{LOAD} |
| t _{PHZ} /t _{PZH} | GND |

| | INPUTS | | | N. | • | - | |
|--------------------------------------|-----------------|--------------------------------|--------------------|-------------------|-------|--------------|--------------|
| V _{CC} | VI | t _r /t _f | VM | V _{LOAD} | C∟ | RL | V_{Δ} |
| $\textbf{1.8 V} \pm \textbf{0.15 V}$ | v _{cc} | ≤2 ns | V _{CC} /2 | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $\textbf{2.5 V} \pm \textbf{0.2 V}$ | Vcc | ≤2 ns | V _{CC} /2 | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |

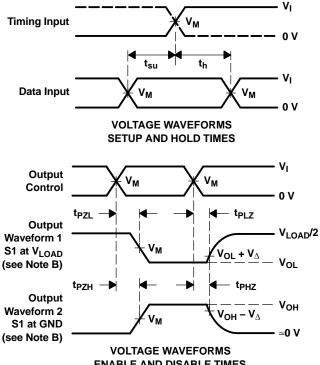


PULSE DURATION



PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS



ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_{L} includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking |
|-----------------------|--------|---------------|------------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|--------------|
| | (1) | (2) | | | (3) | (4) | (5) | | (6) |
| SN74LVC828ADGVR | Active | Production | TVSOP (DGV) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828ADGVR.B | Active | Production | TVSOP (DGV) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828ADW | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC828A |
| SN74LVC828ADW.B | Active | Production | SOIC (DW) 24 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC828A |
| SN74LVC828ADWR | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC828A |
| SN74LVC828ADWR.B | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC828A |
| SN74LVC828APW | Active | Production | TSSOP (PW) 24 | 60 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828APW.B | Active | Production | TSSOP (PW) 24 | 60 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828APWR | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828APWR.B | Active | Production | TSSOP (PW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828APWT | Active | Production | TSSOP (PW) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |
| SN74LVC828APWT.B | Active | Production | TSSOP (PW) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC828A |

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



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PACKAGE OPTION ADDENDUM

23-May-2025

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Texas

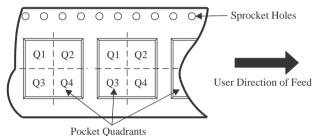
STRUMENTS

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



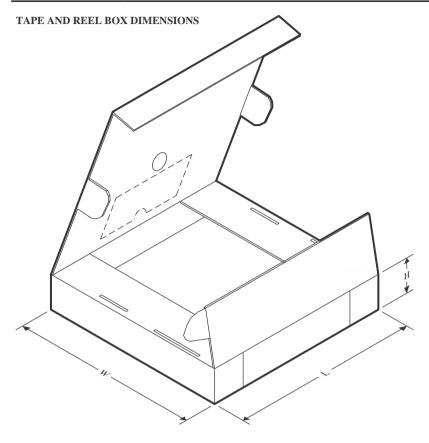
| *All dimensions are nominal | | | | | | | | | | | | |
|-----------------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
| SN74LVC828ADGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC828ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |



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PACKAGE MATERIALS INFORMATION

24-Jul-2025



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC828ADGVR | TVSOP | DGV | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC828ADWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

TEXAS INSTRUMENTS

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24-Jul-2025

TUBE



- B - Alignment groove width

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVC828ADW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVC828ADW.B | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVC828APW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC828APW.B | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



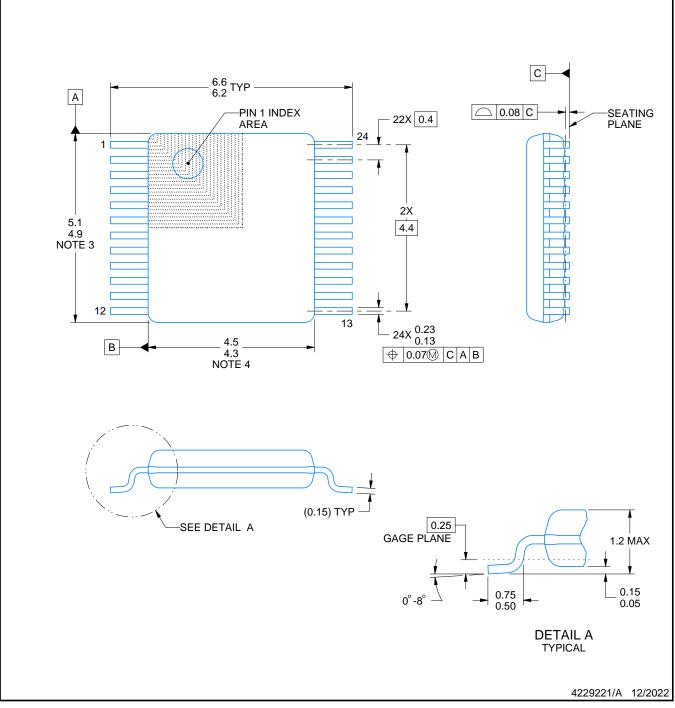
DGV0024A



PACKAGE OUTLINE

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.

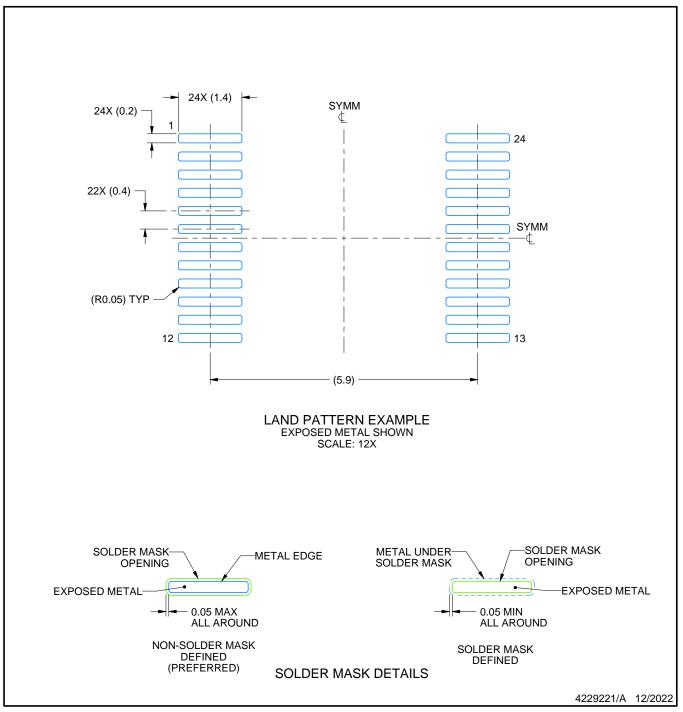


DGV0024A

EXAMPLE BOARD LAYOUT

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

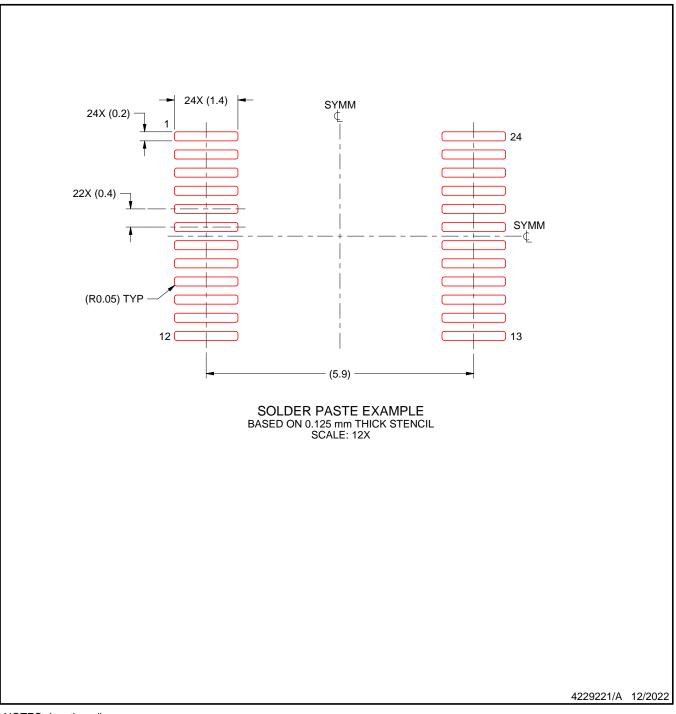


DGV0024A

EXAMPLE STENCIL DESIGN

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0024A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0024A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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