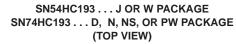
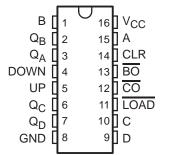
SN54HC193, SN74HC193 **4-BIT SYNCHRONOUS UP/DOWN COUNTERS** (DUAL CLOCK WITH CLEA

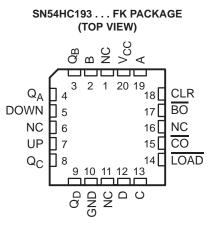
DECEMBER 1982 - REVISED OCTOBER 200

- Wide Operating Voltage Range of 2 V to 6 V
- **Outputs Can Drive Up To 10 LSTTL Loads**
- Low Power Consumption, 80-µA Max ICC
- Typical t_{pd} = 20 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Max





- Look-Ahead Circuitry Enhances Cascaded Counters
- **Fully Synchronous in Count Modes**
- Parallel Asynchronous Load for Modulo-N **Count Lengths**
- **Asynchronous Clear**



NC - No internal connection

description/ordering information

The 'HC193 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

TA	PACKA	GET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC193N	SN74HC193N
		Tube of 40	SN74HC193D	
	SOIC – D	Reel of 2500	SN74HC193DR	HC193
4000 40 0500		Reel of 250	SN74HC193DT	
–40°C to 85°C	SOP – NS	Reel of 2000	SN74HC193NSR	HC193
		Tube of 90	SN74HC193PW	
	TSSOP – PW	Reel of 2000	SN74HC193PWR	HC193
		Reel of 250	SN74HC193PWT	
	CDIP – J	Tube of 25	SNJ54HC193J	SNJ54HC193J
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC193W	SNJ54HC193W
	LCCC – FK	Tube of 55	SNJ54HC193FK	SNJ54HC193FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 2003, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all pa ameters.

SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

description/ordering information (continued)

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

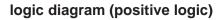
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

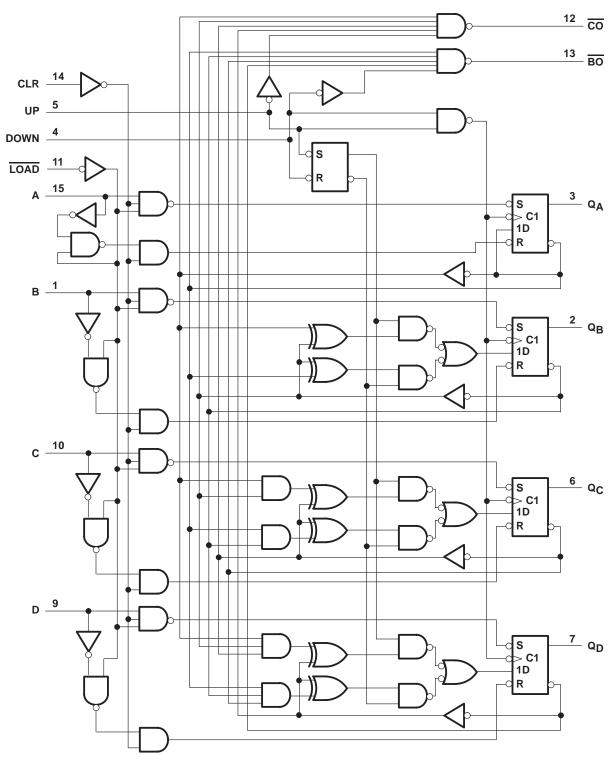
A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and \overline{LOAD} inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow (BO) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry $\overline{(CO)}$ output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding BO and CO to DOWN and UP, respectively, of the succeeding counter.



SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR) SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003





Pin numbers shown are for the D, J, N, NS, PW, and W packages.



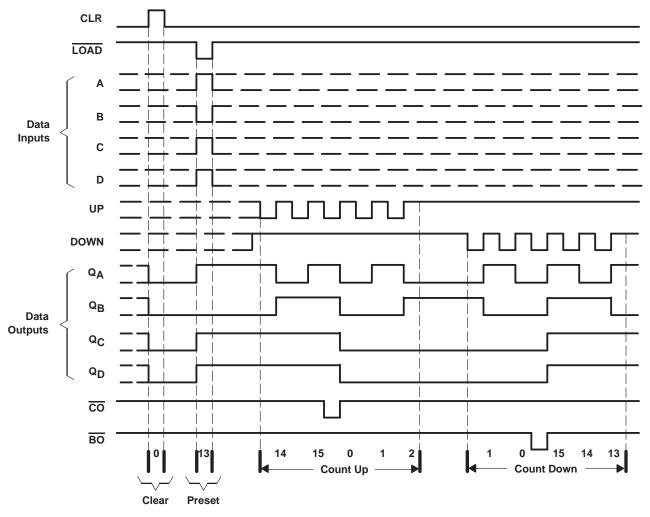
SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

typical clear, load, and count sequence

The following sequence is illustrated below:

- 1. Clear outputs to 0
- 2. Load (preset) to binary 13
- 3. Count up to 14, 15, carry, 0, 1, and 2
- 4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides LOAD, data, and count inputs.B. When counting up, count-down input must be high; when counting down, count-up input must be high.



SN54HC193, SN74HC193 **4-BIT SYNCHRONOUS UP/DOWN COUNTERS** (DUAL CLOCK WITH CLEAR) SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (se Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) Continuous output current, I_O ($V_O = 0$ to V_{CC}) Continuous current through V_{CC} or GND Package thermal impedance, θ_{JA} (see Note 2):	ee Note 1) C) (see Note 1)	±20 mA ±20 mA ±25 mA ±50 mA 73°C/W 67°C/W 64°C/W
Storage temperature range, T _{stg}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN	154HC19)3	SN	174HC19)3	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		$V_{CC} = 2 V$	1.5			1.5			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V
		$V_{CC} = 6 V$	4.2			4.2			
		$V_{CC} = 2 V$			0.5			0.5	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V
		$V_{CC} = 6 V$			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		$V_{CC} = 2 V$			1000			1000	
$\Delta t / \Delta v^{\ddagger}$	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		$V_{CC} = 6 V$			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

[‡] If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at tt = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



SN54HC193, SN74HC193 **4-BIT SYNCHRONOUS UP/DOWN COUNTERS** (DUAL CLOCK WITH CLEAR) SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS			A = 25°C	;	SN54H	IC193	SN74H	C193	
PARAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
∨он	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VOL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
l	$V_I = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000		±1000	nA
ICC	$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160		80	μA
Ci			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				T _A = 1	25°C	SN54F	IC193	SN74H	IC193	
			Vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		4.2		2.8		3.3	
fclock	Clock frequency		4.5 V		21		14		17	MHz
			6 V		24		16		19	
			2 V	120		180		150		
		CLR high	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	120		180		150		
tw	Pulse duration	LOAD low	4.5 V	24		36		30		ns
			6 V	21		31		26		
			2 V	120		180		150		
		UP or DOWN high or low	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	110		165		140		
		Data before LOAD inactive	4.5 V	22		33		28		
			6 V	19		28		24		
			2 V	110		165		140		
t _{su}	Setup time	CLR inactive before UP↑ or DOWN↑	4.5 V	22		33		28		ns
			6 V	19		28		24		
			2 V	110		165		140		
		LOAD inactive before UP↑ or DOWN↑	4.5 V	22		33		28		
			6 V	19		28		24		
			2 V	5		5		5		
^t h	Hold time	Data after LOAD inactive	4.5 V	5		5		5		ns
			6 V	5		5		5		



SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR) SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

	FROM	то		Τį	λ = 25°C	;	SN54H	IC193	SN74H	IC193							
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT						
			2 V	4.2	8		2.8		3.3								
^f max			4.5 V	21	55		14		17		MHz						
			6 V	24	60		16		19								
			2 V		75	165		250		205							
	UP	CO	4.5 V		24	33		50		41							
			6 V		20	28		43		35							
			2 V		75	165		250		205							
	DOWN	BO	4.5 V		24	33		50		41							
4			6 V		20	28		43		35							
^t pd		Any Q	2 V		190	250		375		315 ^{ns}	ns						
	UP or DOWN		Any Q	Any Q	Any Q	4.5 V		40	50		75		63				
			6 V		35	43		64		54							
			2 V		190	260		390		325							
	LOAD	Any Q	4.5 V		40	52		78		65							
			6 V		35	44		66		55							
			2 V		170	240		360		300							
^t PHL	CLR	Any Q	4.5 V		36	48		72		60	ns						
			6 V		31	41		61		51							
			2 V		38	75		110		95							
tt	tt		Any 4	Any 4.	Any	Any	Any	Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16							

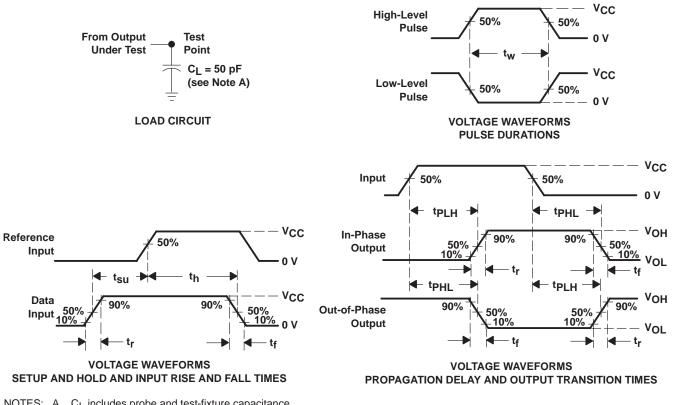
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	50	pF



SN54HC193, SN74HC193 **4-BIT SYNCHRONOUS UP/DOWN COUNTERS** (DUAL CLOCK WITH CLEAR)

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CI includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
- C. For clock inputs, fmax is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.

E. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
						(4)	(5)		
5962-8772401EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J
SN54HC193J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC193J
SN54HC193J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC193J
SN74HC193D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC193
SN74HC193DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193NE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193PW	Obsolete	Production	TSSOP (PW) 16		-	Call TI	Call TI	-40 to 85	HC193
SN74HC193PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SNJ54HC193J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J
SNJ54HC193J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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PACKAGE OPTION ADDENDUM

29-May-2025

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54HC193, SN74HC193 :

• Catalog : SN74HC193

- Automotive : SN74HC193-Q1, SN74HC193-Q1
- Military : SN54HC193

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Military - QML certified for Military and Defense Applications



Texas

STRUMENTS

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC193NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC193PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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PACKAGE MATERIALS INFORMATION

30-Jun-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC193DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC193NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74HC193PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TEXAS INSTRUMENTS

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30-Jun-2025

TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
SN74HC193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193NE4	N	PDIP	16	25	506	13.97	11230	4.32

NS0016A



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- Per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



NS0016A

EXAMPLE BOARD LAYOUT

SOP - 2.00 mm max height

SOP



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NS0016A

EXAMPLE STENCIL DESIGN

SOP - 2.00 mm max height

SOP



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0016A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0016A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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