











SN54HC594, SN74HC594

SCLS040G - DECEMBER 1982-REVISED MARCH 2015

SNx4HC594 8-Bit Shift Registers With Output Registers

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Can Drive up to 15 LSTTL Loads
- Low Power Consumption, 80-μA Maximum I_{CC}
- Typical t_{pd} = 15 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Maximum
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers

2 Applications

- Pro Audio Mixer
- · Elevators and Escalators
- Human Machine Interface (HMI): Industrial Monitor
- Entertainment Systems
- Grid Infrastructure: Grid Control
- Access Control and Security: DVR and DVS

3 Description

The SNx4HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (RCLR, SRCLR) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

The parallel $(Q_A - Q_H)$ outputs have high-current capability. $Q_{H^{'}}$ is a standard output.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
	PDIP (16)	19.30 mm × 6.35 mm		
SN74HC594	COIC (46)	9.00 mm × 9.00 mm		
	SOIC (16)	10.30 mm × 7.50 mm		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)

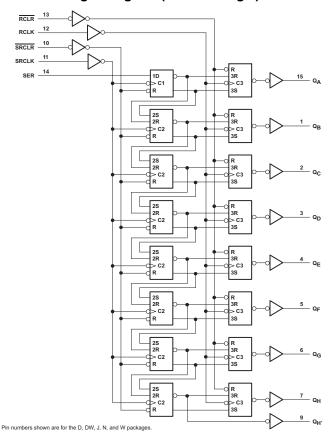




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4 Revision History

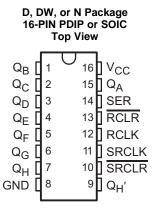
Changes from Revision F (October 2003) to Revision G

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5 Pin Configuration and Functions



Pin Functions

	PIN	1/0	DESCRIPTION
NO.	NAME	I/O	DESCRIPTION
1	Q _B	0	Output B
2	Q _C	0	Output C
3	Q_D	0	Output D
4	Q _E	0	Output E
5	Q _F	0	Output F
6	Q_{G}	0	Output G
7	Q _H	0	Output H
8	GND	_	Ground
9	Q _H	0	Q _H inverted
10	SRCLR	I	Serial clear
11	SRCLK	I	Serial clock
12	RCLK	I	Storage clock
13	RCLK	I	Storage clear
14	SER	I	Serial input
15	Q _A	0	Output A
16	Vcc	-	Power pin



6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$	-20	20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$	-20	20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}	-35	35	mA
	Continuous current through V _{CC} or GND		-70	70	mA
		D package		73	
θ_{JA}	Package thermal impedance (3)	DW package		57	°C/W
		N package		67	
T _{stg}	Storage temperature		-60	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN	54HC594 ⁽²⁾)	SN	174HC594		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	2	5	6	٧
		$V_{CC} = 2 V$	1.5			1.5			
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15			3.15			V
		$V_{CC} = 6 V$	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
V_{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V}$			1.35			1.35	V
		$V_{CC} = 6 V$			1.8			1.8	
VI	Input voltage		0		V _{CC}	0		V _{CC}	V
Vo	Output voltage		0		V_{CC}	0		V_{CC}	٧
		V _{CC} = 2 V			1000			1000	
t _t	Input transition (rise and fall) rate	$V_{CC} = 4.5 \text{ V}$			500			500	ns
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		-55		125	-40		125	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

(2) Product Preview

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.4 Thermal Information

			SN74HC594		
	THERMAL METRIC ⁽¹⁾	N (PDIP)	D (SOIC)	DW (SOIC)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	72.3	71	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	33.2	32.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	29.9	35.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.6	5.3	6.7	
Ψ_{JB}	Junction-to-board characterization parameter	21.1	29.6	35.3	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	ТЕ	EST CONDI	TIONS	V _{CC}	Т	_A = 25°C	;	SN54H -55°C to		SN74H -40°C to		SN74H0 -40°C to		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
				2 V	1.9	1.998		1.9		1.9		1.9		
		I _{OH} = -20 µ	AL	4.5 V	4.4	4.499		4.4		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		5.9		
	$V_{I} = V_{IH}$	Q _H '	$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		3.84		
V _{OH}	or V _{IL}	$Q_A - Q_H$	$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		3.84		V
		Q _H	I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		5.34		
		$Q_A - Q_H$ $I_{OH} = -7.8$ mA		6 V	5.48	5.8		5.2		5.34		5.34		
				2 V		0.002	0.1		0.1		0.1		0.1	
		$I_{OL} = 20 \mu$	١	4.5 V		0.001	0.1		0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1		0.1	
	$V_{I} = V_{IH}$	Q _H '	$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33		0.33	
V _{OL}	or V _{IL}	$Q_A - Q_H$	$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33		0.33	V
		Q _H	I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33		0.33	
		$Q_A - Q_H$	I _{OL} = 7.8 mA	o v		0.15	0.26		0.4		0.33		0.33	
I	$V_I = V_{CC}$	or O		6 V		±0.1	±100		±1000		±1000		±1000	nA
I _{CC}	$V_I = V_{CC}$ or 0,	I _O = 0		6 V			8		160		80		80	μA
C _i				2 V to 6 V		3	10		10		10			pF

⁽¹⁾ Product Preview



6.6 Switching Characteristics: $C_L = 50 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM	TO (OUTDUT)	V _{cc}	T,	₄ = 25°C	;	SN54H0 -55°C to		SN74H		SN74HC -40°C to 1		UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			2 V	5	8		3.3		4		4		
f _{max}			4.5 V	25	35		17		20		20		MHz
			6 V	29	40		20		24		24		
			2 V		50	150		225		185		200	
	SRCLK	$Q_{H'}$	4.5 V		20	30		45		37		42	
•			6 V		15	25		38		31		36	ns
t _{pd}			2 V		50	150		225		185		200	115
	RCLK	$Q_{A} - Q_{H}$	4.5 V		20	30		45		37		42	
			6 V		15	25		38		31		36	
			2 V		50	150		225		185		200	
	SRCLR	$Q_{H'}$	4.5 V		20	30		45		37		42	
t _{PHL}			6 V		15	25		38		31		36	ns
PHL			2 V		50	125		185		155		170	113
	RCLR	$Q_{A} - Q_{H}$	4.5 V		20	25		37		31		36	
			6 V		15	21		31		26		31	
			2 V		38	75		110		95		110	
		$Q_{H'}$	4.5 V		8	15		22		19		21	
t _t			6 V		6	13		19		16		18	ns
प			2 V		38	60		90		75		85	119
		$Q_A - Q_H$	4.5 V		8	12		18		15		17	
			6 V		6	10		15		13		15	

⁽¹⁾ Product Preview

6.7 Switching Characteristics: $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V _{cc}	TA	= 25°C	•	SN54HC -55°C to		SN74H -40°C to		SN74H0 –40°C to		UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			2 V		90	200		300		250		270	
t _{pd}	RCLK	$Q_A - Q_H$	4.5 V		23	40		60		50		55	ns
			6 V		19	34		51		43		48	
			2 V		90	200		300		250		270	
t _{PHL}	RCLR	$Q_A - Q_H$	4.5 V		23	40		60		50		55	ns
			6 V		19	34		51		43		48	
			2 V		45	210		315		265		285	
t _t		$Q_A - Q_H$	4.5 V		17	42		63		53		58	ns
			6 V		13	36		53		45		50	

(1) Product Preview



6.8 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 3	25°C	SN54HC –55°C to	594 ⁽¹⁾ 125°C	SN74H -40°C to	C594 85°C	SN74HC -40°C to		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			2 V		5		3.3		4		4	
f _{clock}	Clock frequer	псу	4.5 V		25		17		20		20	MHz
			6 V		29		20		24		24	
			2 V	100		150		125		130		
		SRCLK or RCLK high or low	4.5 V	20		30		25		27		
	Pulse			17		25		21		23		
t _w	duration		2 V	100		150		125		130		ns
		SRCLR or RCLR low	4.5 V	20		30		25		27		
		6 V	17		25		21		23			
			2 V	90		135		110		115		
		SER before SRCLK↑	4.5 V	18		27		22		24		ns
			6 V	15		23		19		21		
			2 V	90		135		110		115		ns
		SRCLK↑ before RCLK↑ (2)	4.5 V	18		27		22		24		
			6 V	15		23		19		21		
			2 V	50		75		63		68		
t _{su}	Setup time before CLK↑	SRCLR low before RCLK↑	4.5 V	10		15		13		15		
	20.0.0 02.11		6 V	9		13		11		13		
			2 V	20		20		20		20		
		SRCLR high (inactive) before SRCLK↑	4.5 V	10		10		10		10		ns
		OKOLK)	6 V	10		10		10		10		
			2 V	5		5		5		5		
		RCLR high (inactive) before SRCLK↑	4.5 V	5		5		5		5		
		002	6 V	5		5		5		5		
			2 V	5		5		5		5		
t _h	Hold time, SE	R after SRCLK↑	4.5 V	5		5		5		5		ns
			6 V	5		5		5		5		

⁽¹⁾ Product Preview

6.9 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	395	pF

⁽²⁾ This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.



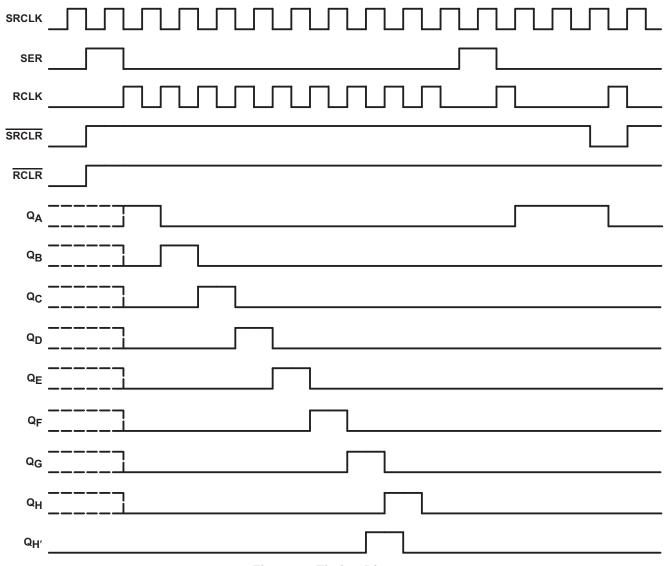
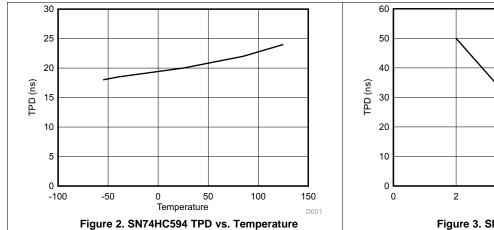
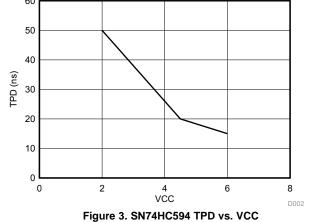


Figure 1. Timing Diagram



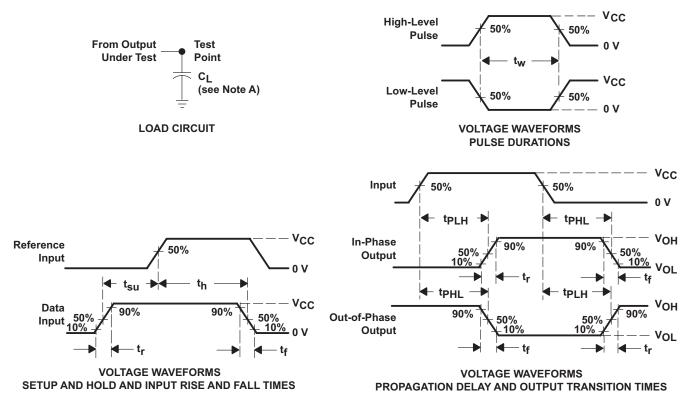
6.10 Typical Characteristics







7 Parameter Measurement Information



- A. C_L includes probe and test-fixture capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. t_f and t_r are the same as t_t .

Figure 4. Load Circuit and Voltage Waveforms



8 Detailed Description

8.1 Overview

The SNx4HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (RCLR, SRCLR) inputs are provided on both the shift and storage registers. A serial (Q_H) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

The parallel (Q_A - Q_H) outputs have high-current capability. Q_H is a standard output.

8.2 Functional Block Diagram

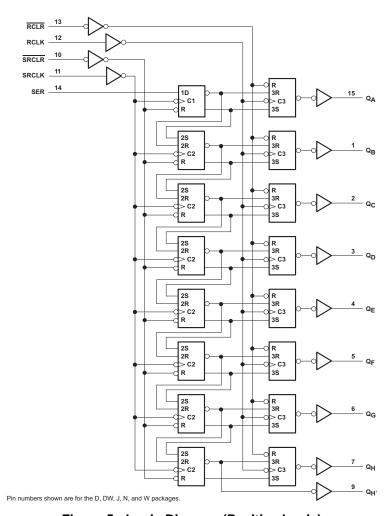


Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The high-current outputs allow the device to drive medium loads without significant drops in output voltage. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.



8.4 Device Functional Modes

Table 1. Function Table

		INPUTS	•		FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	FUNCTION
Χ	Х	L	Χ	Х	Shift register is cleared.
L	1	Н	Х	х	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
Н	1	Н	Х	х	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	Н	Х	Х	Shift register state is not changed.
Χ	X	Χ	Χ	L	Storage register is cleared.
Χ	Х	X	↑	Н	Shift register data is stored in the storage register.
Χ	Х	X	\downarrow	Н	Storage register state is not changed.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC594 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

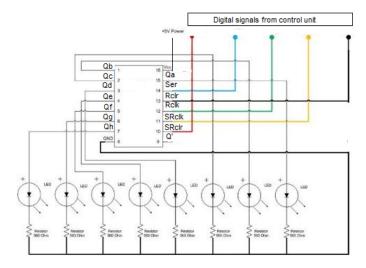


Figure 6. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.



Typical Application (continued)

9.2.2 Detailed Design Procedure

- · Recommended input conditions:
 - Rise time and fall time specs see (Δt/ΔV) in Recommended Operating Conditions table.
 - Specified High and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommended output conditions:
 - Load currents should not exceed 35 mA per output and 70 mA total for the part
 - Outputs should not be pulled above V_{CC}

9.2.3 Application Curves

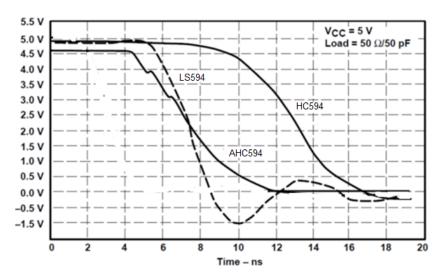


Figure 7. Switching Characteristics Comparison



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

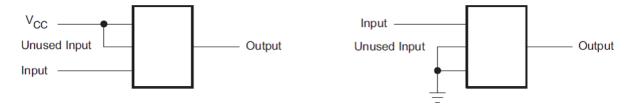


Figure 8. Layout Recommendation



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking	
	(1)	(2)			(3)	Ball material	Peak reflow		(6)	
						(4)	(5)			
SN74HC594D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	HC594	
SN74HC594DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	HC594	
SN74HC594DW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 125	HC594	
SN74HC594DWG4	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DWG4.A	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594DWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	
SN74HC594N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC594N	
SN74HC594N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC594N	

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC594DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC594DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1



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*All dimensions are nominal

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Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74HC594DR	SOIC	D	16	2500	340.5	336.1	32.0	
SN74HC594DR	SOIC	D	16	2500	340.5	336.1	32.0	
SN74HC594DRG4	SOIC	D	16	2500	353.0	353.0	32.0	
SN74HC594DWR	SOIC	DW	16	2000	350.0	350.0	43.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC594DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN74HC594DWG4.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN74HC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC594N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC594N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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