











SN74LVC245A

SCAS218X - JANUARY 1993-REVISED JANUARY 2015

# SN74LVC245A Octal Bus Transceiver With 3-State Outputs

#### **Features**

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 6.3 ns at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)  $> 2 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode and Back Drive protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

### 2 Applications

- Cable Modem Termination Systems
- Servers
- LED Displays
- **Network Switches**
- Telecom Infrastructure
- **Motor Drivers**
- I/O Expanders

### 3 Description

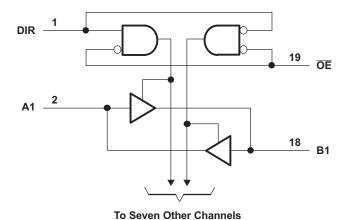
These octal bus transceivers are designed for 1.65-V to 3.6-V V<sub>CC</sub> operation. The 'LVC245A devices are designed for asynchronous communication between data buses.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE
	VQFN (20)	4.50 mm × 3.50 mm
	SSOP (20)	7.50 mm × 5.30 mm
SN74LVC245A	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# **Simplified Schematic**



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.



### **Table of Contents**

1	Features	1	9.1 Overview	9
2	Applications	1	9.2 Functional Block Diagram	9
3	Description		9.3 Feature Description	9
4	Simplified Schematic		9.4 Device Functional Modes	9
5	Revision History	40	Application and Implementation	10
6	Pin Configuration and Functions		10.1 Application Information	10
7	•		10.2 Typical Application	10
1	Specifications	11	Power Supply Recommendations	11
	7.1 Absolute Maximum Ratings	12	Layout	11
	7.2 ESD Ratings 7.3 Recommended Operating Conditions		12.1 Layout Guidelines	
	7.4 Thermal Information		12.2 Layout Example	
	7.5 Electrical Characteristics	12	Device and Documentation Support	
	7.6 Switching Characteristics		13.1 Trademarks	
	7.7 Operating Characteristics		13.2 Electrostatic Discharge Caution	
	7.8 Typical Characteristics		13.3 Glossary	
8	Parameter Measurement Information		Mechanical, Packaging, and Orderable	
9	Detailed Description	9	IIIIOIIIIauoii	12

### 5 Revision History

### Changes from Revision W (May 2013) to Revision X

**Page** 

Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table,
Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation
section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and
Mechanical, Packaging, and Orderable Information section.
 Deleted Ordering Information table.

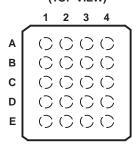
#### Changes from Revision V (September 2010) to Revision W

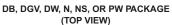
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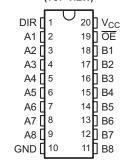


# 6 Pin Configuration and Functions

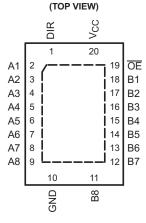








# RGY PACKAGE



### **Pin Functions**

PIN				
NAME	DB, DGV, DW, NS, PW, and RGY	GQN or ZQN	TYPE	DESCRIPTION
A1	2	A1	I/O	Transceiver I/O pin
A2	3	B3	I/O	Transceiver I/O pin
А3	4	B1	I/O	Transceiver I/O pin
A4	5	C2	I/O	Transceiver I/O pin
A5	6	C1	I/O	Transceiver I/O pin
A6	7	D3	I/O	Transceiver I/O pin
A7	8	D1	I/O	Transceiver I/O pin
A8	9	E2	I/O	Transceiver I/O pin
B1	18	B4	I/O	Transceiver I/O pin
B2	17	B2	I/O	Transceiver I/O pin
В3	16	C4	I/O	Transceiver I/O pin
B4	15	C3	I/O	Transceiver I/O pin
B5	14	D4	I/O	Transceiver I/O pin
B6	13	D2	I/O	Transceiver I/O pin
B7	12	E4	I/O	Transceiver I/O pin
B8	11	E3	I/O	Transceiver I/O pin
DIR	1	A2	I	Direction control. When high, the signal propagates from A to B. When low, the signal propagates from B to A.
ŌĒ	19	A4	I	Output enable
GND	10	E1	_	Ground
V <sub>CC</sub>	20	A3	_	Power pin

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### 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or p	power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2)(	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current V <sub>1</sub>	< 0		-50	mA
I <sub>OK</sub>	Output clamp current V <sub>O</sub>	< 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
T <sub>stg</sub>	Sto	orage temperature range	<del>-</del> 65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

	PARAMETER	DEFINITION	VALUE	UNIT
	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	2000	
V <sub>(ESD)</sub>		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

<sup>(2)</sup> The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.



### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			T <sub>A</sub> = 25°C -40°C TO 85°C -40°C TO 125°C							
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
V	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V	
$V_{CC}$	Supply voltage	Data retention only	1.5		1.5		1.5		V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		0.65 × V <sub>CC</sub>			
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		1.7		1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2		2			
$V_{IL}$	Low-level input	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 <b>x</b> V <sub>CC</sub>		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>	.,	
	voltage	$V_{CC}$ = 2.3 V to 2.7 V		0.7		0.7		0.7	V	
		$V_{CC}$ = 2.7 V to 3.6 V		0.8		0.8		8.0		
$V_{I}$	Input voltage		0	5.5	0	5.5	0	5.5	V	
Vo	Output voltage		0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V	
		$V_{CC} = 1.65 \text{ V}$		-4		-4		-4		
1	High-level output	$V_{CC} = 2.3 \text{ V}$		-8		-8		-8	mA	
I <sub>OH</sub>	current	$V_{CC} = 2.7 \text{ V}$		-12		-12		-12	ША	
		$V_{CC} = 3 V$		-24		-24		-24		
		V <sub>CC</sub> = 1.65 V		4		4		4		
1	Low-level output	$V_{CC} = 2.3 \text{ V}$		8		8		8	mA	
l <sub>OL</sub>	current	$V_{CC} = 2.7 \text{ V}$		12		12		12	шд	
		$V_{CC} = 3 V$		24		24		24	1	
$\Delta t/\Delta v$	Input transition rise	or fall rate		10		10		10	ns/V	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### 7.4 Thermal Information

<i>'</i> . ¬	Thermal imormation									
					SN74L	/C245A				
	THERMAL METRIC(1)	DB <sup>(2)</sup>	DGV <sup>(2)</sup>	DW <sup>(2)</sup>	GQN or ZQN <sup>(2)</sup>	N <sup>(2)</sup>	NS <sup>(2)</sup>	PW <sup>(2)</sup>	RGY <sup>(3)</sup>	UNI T
					20 F	PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.5	124.1	92.9	78	59.2	83.6	108.1	44.0	
R <sub>θJC(t</sub>	Junction-to-case(top) thermal resistance	68.1	39.5	60.6		44.9	49.4	43.0	53.0	
R <sub>0JB</sub>	Junction-to-board thermal resistance	61.7	65.5	60.4		40.1	51.2	59.1	22.1	°C/
Ψлт	Junction-to-top characterization parameter	28.5	2.1	28.2		29.9	21.9	4.7	3.0	W
ΨЈВ	Junction-to-board characterization parameter	61.2	64.9	60.0		39.9	50.8	58.6	22.2	
R <sub>θJC(b</sub> ot)	Junction-to-case(bottom) thermal resistance	_	_	_		_	_	_	16.6	

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: SN74LVC245A

<sup>(2)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-5.



#### 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADA	METER	TEST CONDITIONS	V	T <sub>A</sub> =	= 25°C		-40°C TO 8	5°C	-40°C TO 125°C		LINUT	
PAKA	METER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
		Ι <sub>ΟΗ</sub> = -100 μΑ	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V <sub>CC</sub> - 0.2		V <sub>CC</sub> - 0.2			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.29			1.2		1.1			
$V_{OH}$		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.7		1.6		V	
		12 ~ 1	2.7 V	2.2			2.2		2.1			
		$I_{OH} = -12 \text{ mA}$	3 V	2.4			2.4		2.3			
		I <sub>OH</sub> = -24 mA	3 V	2.3			2.2		2.1			
		Ι <sub>ΟL</sub> = 100 μΑ	1.65 V to 3.6 V			0.1		0.2		0.2		
$V_{OL}$		I <sub>OL</sub> = 4 mA	1.65 V			0.24		0.45		0.60	V	
VOL		I <sub>OL</sub> = 8 mA	2.3 V			0.3		0.7		0.75	-	
		I <sub>OL</sub> = 12 mA	2.7 V			0.4		0.4		0.6		
		I <sub>OL</sub> = 24 mA	3 V			0.55		0.55		0.75		
1.	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±1		±5		±10	μΑ	
l <sub>off</sub>		$V_I$ or $V_O = 5.5 \text{ V}$	0			±1		±10		±20	μA	
$I_{OZ}^{(1)}$		V <sub>O</sub> = 0 to 5.5 V	3.6 V			±1		±10		±20	μA	
		$V_I = V_{CC}$ or GND	3.6 V			1		10		30		
I <sub>CC</sub>		$3.6 \text{ V} \le \text{V}_1 \le 5.5 \text{ V}^{(2)}$ $I_0 = 0$	3.0 V			1	10			30	μA	
$\Delta I_{CC}$		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V			500		500		5000	μΑ	
$C_i$ Control inputs $V_I = V_{CC}$ or GND		3.3 V		4						pF		
C <sub>io</sub>	A or B ports <sup>(3)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5.5						pF	

### 7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	-	V <sub>cc</sub>	T	T <sub>A</sub> = 25°C		-40°C TO 85°C		-40°C TO 125°C		UNIT			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX				
			1.8 V ± 0.15 V	1	6	12.2	1	12.7	1	13.7				
	A or B	D A	2.5 V ± 0.2 V	1	3.9	7.8	1	8.3	1	9.1	20			
t <sub>pd</sub>	AUID	B or A	2.7 V	1	4.2	7.1	1	7.3	1	8.3	ns			
			3.3 V ± 0.3 V	1.5	3.8	6.1	1.5	6.3	1.5	7.3				
	ŌĒ					1.8 V ± 0.15 V	1	7	14.8	1	15.3	1	16.8	
		OE A or B	2.5 V ± 0.2 V	1	4.5	10	1	10.5	1	12	ns			
t <sub>en</sub>			2.7 V	1	5.4	9.3	1	9.5	1	11				
			3.3 V ± 0.3 V	1.5	4.4	8.3	1.5	8.5	1.5	10				
			1.8 V ± 0.15 V	1	7.8	16.5	1	17	1	18				
4	ŌĒ	A == D	2.5 V ± 0.2 V	1	4	9	1	9.5	1	10.5				
t <sub>dis</sub>	OE	A or B	2.7 V	1	4.4	8.3	1	8.5	1	9.5	ns			
			3.3 V ± 0.3 V	1.7	4.1	7.3	1.7	7.5	1.7	8.5				
t <sub>sk(o)</sub>			3.3 V ± 0.3 V					1		1.5	ns			

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All typical values are at  $V_{CC}=3.3~V$ ,  $T_A=25~C$ . This applies in the disabled state only. For I/O ports, the parameter  $I_{oz}$  includes the input leakage current.

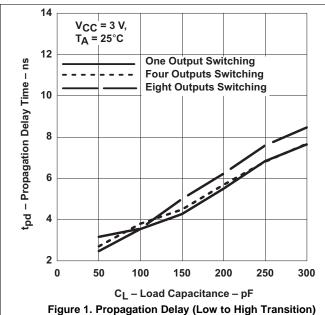


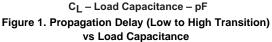
### 7.7 Operating Characteristics

 $T_A = 25^{\circ}C$ 

	PARAMETER		TEST CONDITIONS	V <sub>cc</sub>	TYP	UNIT
			f = 10 MHz	1.8 V	42	
	Power districts of the second	Outputs enabled		2.5 V	43	pF
				3.3 V	45	
$C_{pd}$	Power dissipation capacitance per transceiver			1.8 V	1	
		Outputs disabled		2.5 V	1	
				3.3 V	2	

### 7.8 Typical Characteristics





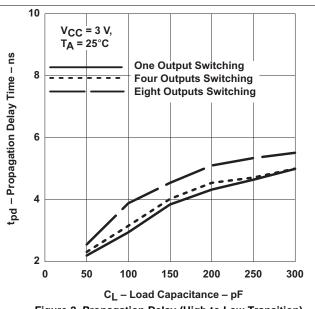
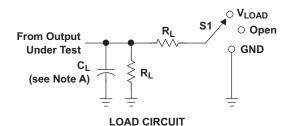


Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

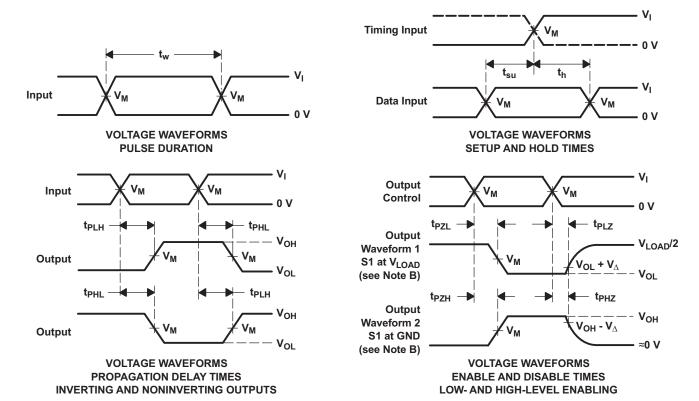


### 8 Parameter Measurement Information



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$V_{LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V	INF	PUTS	V	V V			V
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub> V <sub>LOAD</sub>		CL	$R_L$	$oldsymbol{V}_{\Delta}$
1.8 V ± 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	Vcc	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	<b>500</b> Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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### 9 Detailed Description

#### 9.1 Overview

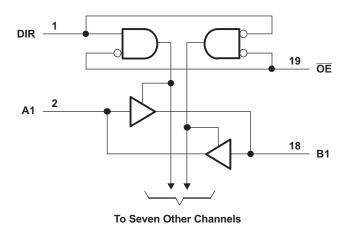
This octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC245A device is designed for asynchronous communication between data buses. This device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses effectively are isolated.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 9.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

#### 9.3 Feature Description

- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V

#### 9.4 Device Functional Modes

**Table 1. Function Table** 

INF	PUTS	OPERATION					
ŌĒ	DIR	OFERATION					
L	L	B data to A bus					
L	Н	A data to B bus					
Н	X	Isolation					

Product Folder Links: SN74LVC245A



### 10 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

SN74LVC245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation.

### 10.2 Typical Application

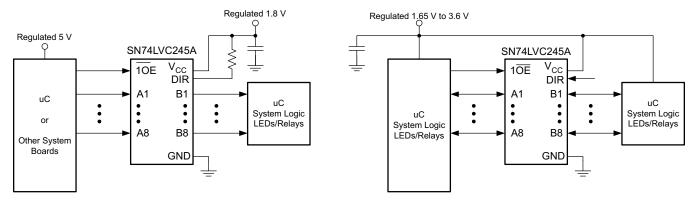


Figure 4. Typical Application Schematic

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in the Recommended Operating Conditions table.
  - For specified high and low levels, see (V<sub>IH</sub> and V<sub>IL</sub>) in the Recommended Operating Conditions table.
  - Inputs are overvoltage tolerant allowing them to go as high as (V<sub>1</sub> max) in the Recommended Operating
     Conditions table at any valid V<sub>CC</sub>.

### 2. Recommend Output Conditions

Load currents should not exceed (I<sub>O</sub> max) per output and should not exceed (Continuous current through V<sub>CC</sub> or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

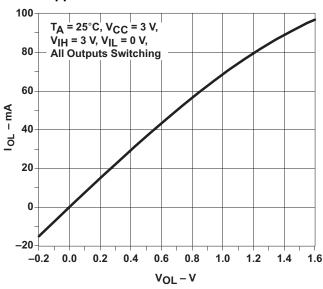
Product Folder Links: SN74LVC245A

Outputs should not be pulled above V<sub>CC</sub>.



### **Typical Application (continued)**

#### 10.2.3 Application Curves



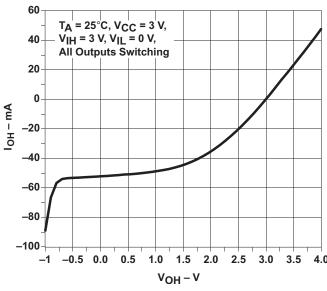


Figure 5. Output Drive Current (I<sub>OL</sub>) vs LOW-level Output Voltage (V<sub>OL</sub>)

Figure 6. Output Drive Current (I<sub>OH</sub>) vs HIGH-level Output Voltage (V<sub>OH</sub>)

### 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu$ F capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01  $\mu$ F or 0.022  $\mu$ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

### 12 Layout

#### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

#### 12.2 Layout Example



Figure 7. Layout Diagram



### 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

### 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Product Folder Links: SN74LVC245A

www.ti.com

17-Jun-2025

### **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC245ADBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADBRE4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADBRG4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVR	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVR.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVRG4	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVRG4.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWRG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245AN.B	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245ANE4	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245ANS.B	Active	Production	SOP (NS)   20	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSRG4	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSRG4.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245APW	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWE4	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWG4	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRE4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG3	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC245A



-40 to 125

-40 to 125

17-Jun-2025

LC245A

LC245A



SN74LVC245ARGYRG4

SN74LVC245ARGYRG4.B

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Orderable part number	Status	Material type (2)	Package   Pins	Package qty   Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVC245APWRG3.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG4.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWT	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWT.B	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ARGYR	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A
SN74LVC245ARGYR.B	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A

Yes

Yes

NIPDAU

NIPDAU

Level-2-260C-1 YEAR

Level-2-260C-1 YEAR

Active

Active

3000 | LARGE T&R

3000 | LARGE T&R

Production

Production

VQFN (RGY) | 20

VQFN (RGY) | 20

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

### PACKAGE OPTION ADDENDUM

www.ti.com 17-Jun-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVC245A:

● Enhanced Product : SN74LVC245A-EP

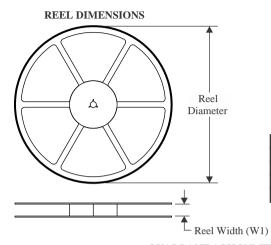
NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications



www.ti.com 24-Jul-2025

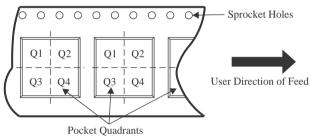
### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC245ADGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC245ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LVC245ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC245ANSRG4	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74LVC245ARGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



www.ti.com 24-Jul-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC245ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVC245ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC245ADGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVC245ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC245ANSRG4	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC245APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC245APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC245APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC245APWT	TSSOP	PW	20	250	353.0	353.0	32.0
SN74LVC245ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74LVC245ARGYRG4	VQFN	RGY	20	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC245ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC245AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245ANE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245ANS.B	NS	SOP	20	40	530	10.5	4000	4.1
SN74LVC245APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



### DGV (R-PDSO-G\*\*)

### **24 PINS SHOWN**

### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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